Fonds Steina et Woody Vasulka

- [Vasulka, Woody] ; [Schier, Jeffy] ; [Moxon, Tom]. — The articulator manual. — [ca. 1977]. — [81] p. — Guide d'utilisation non publié du «Digital Image Articulator». — Sortie d'imprimante.

Steina and Woody Vasulka fonds

- [Vasulka, Woody] ; [Schier, Jeffy] ; [Moxon, Tom]. — The articulator manual. — [ca. 1977]. — [81] p. — Unpublished instruction manual of the «Digital Image Articulator». — Computer printout.

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THE ARTICULATOR MANUAL.TIF

THE ARTICULATOR MANUAL

THE VASULKA IMAGING SYSTEM

A SHORT OVERVIEW

OUR DIGITAL VIDEO SYSTEM IS A MICROPROGRAMMABLE PROCESSOR FOR THE AQUISITION, STORAGE, MODIFICATION AND DISTRIBUTION OF DIGITALLY ENCODED VIDEO OF FOUR BIT RESOLUTION. IT CONSISTS OF THE FOLLOWING SUBSECTIONS:

- QUANTIZERS (ANALOG/DIGITAL CONVERTERS)
- BUFFERS
- MICROPROGRAMMED MICROPROCESSOR
- INTERFACE TO DEC LSI-11 MICROCOMPUTER
- BUFFER AND SCREEN ADDRESSING CIRCUITRY
- OUTPUT SELECTION LOGIC
- DIGITAL TO ANALOG RECONVERSION

DIGITAL IMAGE PROCESSING IS THE TERM APPLIED TO THE NUMERICAL CODIFICATION AND SUBSEQUENT ALGORITHMIC MANIPULATION OF PICTORIAL INFORMATION. THIS CODIFICATION OR Q U A N T I Z - A T I O N OF THE IMAGE IS PERFORMED ON A POINT BY POINT BASIS AS THE PICTURE IS SCANNED, ASSIGNING A NUMBER TO EACH POINT CORRESPONDING TO THE LUMINANCE VALUE OF THE PICTURE AT THAT POINT. THE RANGE OF NUMBERS THAT MAY BE ASSIGNED TO EACH POINT, DETERMINE THE AMOUNT OF DISCRETE INTENSITY CHANGES, THAT MAY BE DETECTED; WHILE THE NUMBER OF INDIVIDUAL POINTS DETERMINE THE SMALLEST AREA OF THE PICTURE THAT MAY BE ENCODED.

THIS QUANTIZATION IS IMPLEMENTED BY A REAL-TIME DIGITAL CONVERSION OF THE TELEVISION (ANALOG) SIGNAL, WHERE THE DIGITAL WORD SIZE CORRESPONDS TO THE RANGE OF NUMBERS WHICH MAY BE ASSIGNED, AND THE ANALOG SAMPLING RATE DETERMINES THE NUMBER OF INDIVIDUAL POINTS THAT MAY BE RESOLVED FROM THE ORIGINAL PICTURE.

FRAME BUFFER PROCESSING IS THE TERM APPLIED TO THE STORAGE OF SINGLE FRAMES, OR SEQUENCES OF FRAMES, ALLOWING TRANSFORMATIONS OF PIXEL LOCATION WITHIN A FRAME, OR OVER A NUMBER OF FRAMES. IN OUR SYSTEM, WE HAVE EIGHT IMAGE BUFFERS OF 8K DEEP BY FOUR BITS WIDE, WITH HIGH SPEED (200 NS) ACCESS TIME. ENTERING EACH BUFFER ARE FOUR BUSSES CARRYING CONTROL SIGNALS, ADDRESS AND DATA INFORMATION. AT ANY TIME, ANY BUFFER MAY BE CONNECTED TO ANY ONE OF THE FOUR BUSSES. THIS ALLOWS FOR EXPANSION OF THE IMAGE RESOLUTION BY CONCATENATION OF SEVERAL BUFFERS ONTO THE SAME BUS. FOR EXAMPLE, CONNECTING TWO BUFFERS TO THE SAME BUS, MAKES THEM APPEAR TO THE BUS AS A WIDENED 8K BY 8 BIT BUFFER. CONNECTION OF A PARTICULAR BUFFER TO A BUS IS INITIATED BY THE BUFFER PRIORITY LOGIC ASSOCIATED WITH EACH BUFFER.

A HIGH SPEED (200 NS) MICROPROCESSOR, BASED ON THE AMD 2900 BIT SLICE INTEGRATED CIRCUIT, IS CONNECTED TO TWO OF THE FOUR BUSSES THAT FEED THE IMAGE BUFFERS. BY CONRTOLLING THE TWO BUSSES, READING AND WRITING MAY BE DONE TO DIFFERENT LOCATIONS IN TWO DIFFERENT BUFFERS. THIS GIVES THE CAPABILITY OF VARIOUS PICTURE TRANSFORMATIONS, SUCH AS PICTURE INVERSION, COMPRESSION, EXPANSION, EDGE EXTRACTION, AND OUTLINING.

A SEQUENCER AND A 256 WORD PROGRAM CONTROL STORE GIVE INSTRUCTION TO THE MICROPROCESSOR, WHICH IS STRUCTURED AROUND AN 80 BIT PIPELINE. THIS CONTROL STORE HAS THE CAPABILITY FOR EXPANSION UP TO 4096 WORDS.

THIS ARRANGEMENT BRINGS 80 BIT LONG CODE, DIVIDED INTO FUNCTIONAL FIELDS, SERVICING INTERNAL DEVICES IN EVERY 200 NS. IN SIMPLE OPERATIONS, THE INTEGRITY OF A REAL TIME PERFORMANCE IS PRESERVED.

THE INTERFACE CONNECTS THE LSI-11 MICROCOMPUTER TO THE MICROPROCESSOR AND THE BUFFERS. A BUFFER REQUEST REGISTER IS ON THE INTERFACE, TO ALLOW REQUESTS FOR USAGE OF A PARTICULAR BUFFER.

BUFFER AND SCREEN ADDRESSING CIRCUITRY ACCOMODATES THE GENERATON OF THE HORIZONTAL AND VERTICAL TIMING, TO SCAN OUT OR WRITE IN DIGITIZED VIDEO INFORMATION TO THE IMAGE BUFFERS, ALTERING THE HEIGHT AND WIDTH OF THE PICTURE, SHIFTING THE POSITION OF THE SCREEN AND PIXEL REMAPPING. THE PHASE OF THE HIGH FREQUENCY CLOCK IS LOCKED TO THE VIDEO SUBCARRIER PHASE TO AVOID COLOR SHIFTS IN THE SYSTEM. THE TIMING OF THE X/Y TIMING CHAIN DETERMINING THE PIXEL COORDINATES, IS IN TURN LOCKED TO THIS HIGH FREQUENCY CLOCK. THE HIGH FREQUENCY CLOCK ITSELF SETS THE TIME-GRID WHICH SPECIFIES THE MAXIMUM AND MINIMUM RESOLUTION ATTAINABLE IN THE SCANNING OF THE BUFFERS. WITH A HIGH FREQUENCY CLOCK OF 9.75524 MHZ AND AN ACTIVE VIDEO LINE OF 52.4 MICROSECOND DURATION, THIS FORMS A TOTAL NUMBER OF 512 PICTURE ELEMENTS FOR HORIZONTAL RESOLUTION. HOWEVER, DUE TO THE BUFFER CYCLE TIME OF 200 NS., BUFFER IMAGE RESOLUTION IS FURTHER LIMITED TO 256 PIXELS. THUS, TO STORE A 256 BY 256 IMAGE REQUIRES SOME 65,536 MEMORY LOCATIONS, WHICH IS JUST THE SIZE OF OUR COMPLETE BUFFER MEMORY. BY GROUPING ALL EIGHT BUFFERS, ONE FRAME OF 256 BY 256 BY 4 RESOLUTION MAY BE STORED, BUT MORE FRAMES CAN BE STORED IF A LOWER RESOLUTION IS USED. FOR INSTANCE, IF 128 BY 128 RESOLUTION IS USED THEN FOUR FRAMES MAY BE STORED IN A SEQUENCE, AND IF 128 BY 64 RESOLUTION IS USED THEN EIGHT CAN BE STORED.

DISCNAME: 0
DISCNAME: OVERV
UPDATED: 25-NOV-80

IMAGE EMULSIFIER

THE IMAGE EMULSIFIER CONSISTS OF AT LEAST FOUR DISTINCT SUBSECTIONS:

A) EIGHT IMAGE BUFFERS
B) A HIGH SPEED MICRO-PROGRAMMED PROCESSOR
C) AN X/Y ADDRESS FORMATION CIRCUITRY
D) A MICRO-COMPUTER INTERFACE

A) EIGHT IMAGE BUFFERS OF 8K BY 4 BIT SIZE:

THESE BUFFERS ARE CONTAINED ON TWO WIRE-WRAP CARDS, FOUR BUFFERS TO A CARD. FOUR BUSES ENTER EACH BUFFER CARD, CARRYING ADDRESS INFORMATION (14 BITS, OF WHICH 13 BITS ARE USED), DATA (4 BITS WIDE), AND CONTROL SIGNALS (TWO BITS); ONE FOR 'BUFFER CHIP ENABLE' THE OTHER A READ/WRITE LINE. AT ANY ONE TIME, A BUFFER MAY BE CONNECTED TO ANY ONE OF THE FOUR BUSES. CONNECTING TWO OF THE 8K BUFFERS TO THE SAME BUS MAKES THE TWO BUFFERS APPEAR AS A WIDENED 8K BY 8 BIT BUFFER. CONNECTING FOUR OF THE BUFFERS TO THE SAME BUS WIDENS THE BUFFER WORD TO 8K WORDS BY 16 BITS. CONNECTION OF A PARTICULAR BUFFER TO A BUS IS INITIATED BY THE BUFFER PRIORITY LOGIC. 8K BY 4 ALLOWS FOR A 128 BY 64 PIXEL IMAGE. BY TIME INTERLEAVING OF TWO 8K BY 4 BUFFERS, A 128 BY 128 PIXEL IMAGE MAY BE FORMED. THIS INTERLEAVING IN TIME, FREES ONE BUFFER FOR PROCESSING, WHILE THE OTHER IS USED TO THE IMAGE DISPLAY TIMING; ALMOST THE ENTIRE FIELD TIME IS FREED FOR PROCESSING. THIS COULD BE ARRANGED BY ASSIGNING ONE BUFFER TO THE TOP HALF OF THE SCREEN AND ANOTHER BUFFER TO THE LOWER HALF OF THE SCREEN. WHILE THE TOP HALF OF THE SCREEN IS BEING DISPLAYED THE LOWER HALF OF THE SCREEN'S BUFFER MAY BE USED FOR PROCESSING. THE SWITCH-OVER POINT WILL OCCUR DURING HORIZONTAL BLANKING AFTER 120 VISIBLE LINES ARE DISPLAYED (SAY LINE 141 OF THE ODD OR EVEN FIELD, ASSUME 21 LINES OF VERTICAL BLANKING AND THE SAME LINE NUMBERING IS APPLIED TO EACH VIDEO FIELD).

REQUEST OF THE SWITCH-OVER IS MADE BY THE ADDRESSING LOGIC, REQUESTING USE OF THE LOWER BUFFER. IF THE X-Y ADDRESSING IS ASSIGNED THE HIGHEST PRIORITY, IT WILL BE GRANTED USAGE AFTER ONE MEMORY CYCLE (200 NANOSECONDS). ONCE GRANTED USAGE OF THE LOWER SCREEN BUFFER, THE ADDRESSING LOGIC RELEASES USE OF THE UPPER BUFFER BY NEGATING ITS REQUEST LINE FOR THE UPPER BUFFER. THIS FREES THE UPPER BUFFER FOR OTHER UNITS' USAGE, E.G. THE CPU, HIGH SPEED PROCESSOR, ETC. PROCESSING MAY NOW BE DONE UPON THE TOP BUFFER AFTER REQUEST OF ITS USE.

ANOTHER SUBTLE FEATURE OF EACH IMAGE BUFFER IS THAT DURING A WRITE OPERATION, THE DATA PRESENT AT THE IMAGE BUFFERS' DATA INPUT CAN BE LOOPED THROUGH TO THE OUTPUT LATCH. THE OUTPUT FROM THE BUFFER, AT THE END OF THE MEMORY WRITE CYCLE, IS THE DATA WRITTEN INTO THE BUFFER. VERIFICATION OF THE WRITE OPERATION MAY BE ACHIEVED BY FOLLOWING THE WRITE CYCLE WITH A READ CYCLE. THIS LOOP-AROUND FEATURE PREVENTS SPURIOUS DATA OUTPUT DURING A WRITE CYCLE. DURING A WRITE OPERATION, THE OUTPUT MAY STILL BE USED FOR FURTHER PROCESSING OR VIEWING WHILE THE BUFFER ACQUIRES NEW INFORMATION. THIS IS ESPECIALLY USEFUL IN FRAME GRABBING APPLICATIONS, WHEN NEW DATA IS PUSHED INTO THE FRAME BUFFER, WHILE OUTPUT DATA IS BEING SENT TO THE DISPLAY.

b) A HIGH SPEED (200 NS) MICRO-PROGRAMMED PROCESSOR:

THIS PROCESSOR IS CONNECTED TO TWO OF THE FOUR BUSES THAT FEED THE BUFFERS. BY CONTROLLING TWO BUSES, THE PROCESSOR CAN READ/WRITE DIFFERENT ADDRESSES IN TWO SEPARATE BUFFERS. THIS IS USEFUL FOR VARIOUS IMAGE TRANSFORMATIONS, SUCH AS IMAGE INVERSION, COMPRESSION AND EDGE EXTRACTION. PROCESSING MAY BE DONE TO DIFFERENT PORTIONS OF THE IMAGE, DURING ONE PROCESSOR CYCLE. TIME DELAYS BECOME AN IMPORTANT FACTOR IN PROCESSING INFORMATION IN TWO SEPARATE BUFFERS. A DELAY OF ONE MEMORY CYCLE TIME WILL BE EXPERIENCED, FROM THE REQUEST OF THE READ CYCLE UNTIL THE DATA IS AVAILABLE AT THE BUFFER OUTPUT. A WRITE CYCLE TO A BUFFER REQUIRES DATA TO BE PRESENT AT THE BEGINNING OF THE CYCLE, AND IS WRITTEN IN DURING THE CYCLE. AT FULL SPEED OPERATION, THE PROCESSOR ALSO EXHIBITS A 200 NANOSECOND DELAY FROM INPUT TO OUTPUT. THESE TIME DELAYS ARE INHERENT IN A LATCHED SYSTEM, AND CAN BE ACCOMODATED THROUGH SHIFTING FORWARD READ OPERATIONS AND SHIFTING BACK THE WRITE OPERATIONS IN TIME. THIS IS A FORM OF 'PREPARING AHEAD' TO SYNCHRONIZE READ AND WRITE OPERATIONS.

C) AN X/Y ADDRESS FORMATION CIRCUITRY:

THIS SECTION GENERATES THE HORIZONTAL AND VERTICAL TIMING SIGNALS TO SCAN OUT, OR WRITE IN DIGITIZED VIDEO INFORMATION FOR THE IMAGE BUFFERS. MODULATION OF THE X/Y SIGNALS ALLOWS A CONTINUOUS MODULATION OF THE BUFFER SCANNING, CREATING SIMILAR EFFECTS AS IN SCAN PROCESSING; A MODULATION OF THE DEFLECTION SIGNALS, RESULTING IN SCREEN COMPRESSION OR EXPANSION, ADJUSTMENT OF HEIGHT AND WIDTH, AND SHIFTS IN THE SCREEN POSITION ALONG THE HORIZONTAL AND VERTICAL AXES.

A PRELIMINARY CONSTRAINT WILL BE TO LOCK THE TIMING OF THE X-Y TIMING CHAIN TO A CONSTANT HIGH FREQUENCY CLOCK. THE A HIGH FREQUENCY CLOCK, DRIVING THE X-Y TIMING CHAIN, DETERMINES A 'TIME GRID' SPECIFYING THE MAXIMUM AND MINIMUM RESOLUTION ATTAINABLE BY SCANNING OF THE BUFFERS. THE BUFFERS DETERMINE THE SMALLEST TIME INTERVAL, WHICH IS THE BUFFER CYCLE TIME OF 200 NANOSECONDS. WITH A VISIBLE (OR ACTIVE) LINE OF 52.4 MICROSECONDS, A TOTAL OF 256 PIXELS MAY BE SCANNED OUT PER LINE BY USE OF ONE BUFFER. THIS 200 NANOSECONDS TIME INCREMENT ESPECIALLY EFFECTS PICTURE COMPRESSION. IF A 128 BY 128 IMAGE IS COMPRESSED, ITS SMALLEST SIZE RETAINING ALL THE POINTS (PIXELS) WOULD BE COMPRESSION TO HALF SIZE ALONG THE VERTICAL AND HORIZONTAL AXES. FURTHER COMPRESSION INVOLVES THE 'SKIPPING' OR INTERPOLATION OF IMAGE DATA. AN EXAMPLE WOULD BE COMPRESSING THE BUFFERS SCANNING WITHIN AN 87 BY 87 GRID (87 PIXELS ON THE HORIZONTAL BY 87 ON THE VERTICAL). THIS TAKES UP 17.4 MICROSECONDS OR ABOUT ONE THIRD OF SCREEN SIZE. ONLY 87 POINTS BY 87 POINTS MAY BE DISPLAYED OUT OF THE POSSIBLE 128 BY 128. THE HORIZONTAL AXIS NOW LIMITS RESOLUTION IN A SIMILAR WAY TO THE VERTICAL'S LINE STRUCTURE. BY IMPOSING THIS 'TIME GRID' WE HAVE TO FIT IMAGES INTO THE RESOLUTION OF THIS GRID. THE DETERMINATION OF WHICH POINTS TO 'SKIP' OR INTERPOLATE IS A QUESTION WHICH WILL HAVE TO BE EMPIRICALLY VERIFIED (OR GUESSED AT), TO ACHIEVE SMOOTH COMPRESSION OF AN IMAGE BETWEEN SUCCESSIVE FIELDS. DEVELOPMENT OF ALGORITHMS TO ACHIEVE THIS ZOOMING OR SQUEEZING OF IMAGE IS ANOTHER CONSIDERATION.

SPATIAL RANDOMNESS CAN BE ACHIEVED BY INJECTING PSEUDO RANDOM NOISE INTO THE ADDRESSING LOGIC BY ADDITION, MULTIPLICATION OR A BINARY/BOOLEAN OPERATION. THESE NOISE GENERATORS CAN ALSO BE A SOURCE FOR FAST DATA DEGRADATION WHEN PROCESSING BUFFER DATA CONTENTS.

D) A MICRO-COMPUTER INTERFACE:

THIS INTERFACE CONNECTS THE LSI-11 TO THE VIDEO PROCESSOR AND TO ONE BUS OF THE IMAGE BUFFERS. A BUFFER REQUEST REGISTER IS ON THE INTERFACE TO ALLOW REQUESTS FOR USAGE OF A PARTICULAR BUFFER. THE LSI-11 MUST FIRST REQUEST USAGE TO ACCESS DATA OF A BUFFER. IF IT IS THE HIGHEST PRIORITY DEVICE, A GRANT REGISTER WILL INDICATE THAT IT HAS USAGE OF THE BUFFER (THE REQUEST WAS GRANTED). THIS GRANT REGISTER CAN BE ENABLED TO GENERATE INTERRUPTS UPON GETTING A BUFFER. ONCE A BUFFER REQUEST/GRANT SEQUENCE IS SUCCESSFUL A 1K BLOCK OF DATA MAY BE WRITTEN IN, OR READ FROM THE GRANTED BUFFER. TO WRITE TO THE OTHER SECTIONS OF THE BUFFER A MEMORY PAGE REGISTER IS USED TO MAP THE 1K MEMORY SPACE INTO ONE OF THE PAGES OF THE 8K BUFFER.

THE LSI-11 IS ALSO RESPONSIBLE FOR SETTING THE BUFFER PRIORITY REGISTERS ON THE EIGHT IMAGE BUFFERS. THE CPU MUST MONITOR THE BUFFER ACTIVITY TO TIME ITS CHANGE OF PRIORITY. IT IS PROBABLE, THAT THE BUFFER PRIORITY LOGIC WILL ALLOW THE PRIORITY TO BE CHANGED; THIS WILL AFFECT THE NEXT MEMORY CYCLE, ALLOWING THE CURRENT DEVICE TO HAVE CONTROL UNTIL THE PRIORITIES HAVE BEEN CHANGED. A CONTROL REGISTER FOR THE OPERATION OF WRITABLE CONTROL STORE, CONTROLS THE RUN/SINGLE STEP/STOP OF THE VIDEO PROCESSOR AND OTHER FUNCTIONS, NEEDED TO CONSTRUCT MICRO-PROGRAMS TO DEVELOPE IMAGING ALGORITHMS.

DISCNAME: 0
FILENAME: RASTER
UPDATED: 25-OCT-79

VIDEO PROCESSING AND BUFFERING

IN RASTER SCAN GRAPICS TWO SCHOOLS OF THOUGHT ARE PREVALENT WHEN DEALING WITH IMAGE FORMATION. ONE IS THE PROCESSING VIEW, WHERE SIGNALS ARE SEEN AS REAL-TIME SIGNALS THAT MAY BE DELAYED, MODIFIED OR SWITCHED, BUT MUST CONFORM TO THE RESTRICTIONS OF "REAL-TIME." THE OTHER APPROACH IS THE BUFFER OR STORAGE MODE, WHERE INFORMATION IS TAKEN IN AND STORED AS SEQUENCES OF STILL PHOTOGRAPHS AND REPLAYED OR RECALCULATED AS A MEMORY ARRAY.

PROCESSING REQUIRES HIGH SPEED; OFTEN ACCOMPLISHED THROUGH USE OF FAST, RELATIVELY SIMPLE PROCESSING UNITS, WHICH ARE ITERATIVELY COMBINED TO PROCESS THE SIGNAL. INFORMATION STORAGE IS OF A SHORT FORM VARIETY AND PIPELINING OR ARRAY PROCESSING ALLOWS FOR COMPLEX OPERATIONS TO BE FORMED BY COLLECTIONS OF THESE PROCESSING MODULES.

THE BUFFER APPROACH UTILIZES A DUAL-PORTED MEMORY ARRAY OF A LARGE SIZE TO STORE THE IMAGE. THE DISPLAY SCREEN IS "BACKED UP" BY THIS MEMORY ARRAY, WITH THE ADDRESSING CORRESPONDING TO HORIZONTAL AND VERTICAL POSITION ON THE SCREEN. FOR A 640 X 480 ELEMENT DISPLAY, WE REQUIRE 307,2000 WORDS OF MEMORY PER FRAME, WITH THE WORD LENGTH CORRESPONDING TO GREY SCALE AND/OR COLOR RENDITION. THIS LARGE SIZE IMAGE BUFFER IS OFTEN CALLED A "FRAME BUFFER," AND IS VIEWED AS A "RAM INTENSIVE APPLICATION", WHEN DESCRIBED BY THE SEMICONDUCTOR INDUSTRY.

UTILIZATION OF THIS DENSE MEMORY MUST BE CAREFULLY EXAMINED IF IT IS TO BE EFFICIENTLY UTILIZED. 75% OF THE TOTAL MEMORY ACCESS IS DEDICATED TO ITS SCANNING FOR A TELEVISION TYPE RASTER: FROM LEFT TO RIGHT AND TOP TO BOTTOM.

DISCNAME: 0
FILENAME: PIXARI
UPDATED: 13-JAN-79

P I X E L A R I T H M E T I C

ADDRESSING AND SCREEN POSITIONS:

THIS IS A DESCRIPTION OF THE NUMBERING SCHEME FOR RELATING BUFFER ADDRESSES TO THEIR CORRESPONDING SCREEN POSITIONS, WHEN SENT FOR DISPLAY TO THE TELEVISION RASTER.

THE IMAGE BUFFERS ARE AN 8K (8192) ADDRESS BY 4-BIT-WIDE BLOCKS OF MEMORY. EACH OF THESE 8192 LOCATIONS IS ADDRESSED IN A LINEAR SEQUENCE, FROM ZERO (Ø) THROUGH 8191. THE X-Y ADDRESSING SCHEME DETERMINES HOW THESE LOCATIONS ARE MAPPED TO SPECIFIC SCREEN POSITIONS, WHEN USED FOR OUTPUT.

CERTAIN CONVENTIONS ARE USEFUL WHEN UTILIZING THESE BUFFERS FOR ACQUISITION OF DIGITIZED VIDEO SIGNALS, AND WHEN COMPOSING HIGHER DENSITY (GREATER NUMBER OF PIXEL ELEMENTS) IMAGES. FOR A 128 BY 128 PIXEL DISPLAY TWO BUFFERS ARE USED, ONE ASSIGNED TO THE TOP HALF OF THE SCREEN THE OTHER TO THE BOTTOM HALF. EACH BUFFER DISPLAYS 64 LINES OF 128 PIXEL PER LINE. THIS MODE IS CALLED OUR 'STANDARD VERTICAL SPLIT' MODE OF OPERATION.

PLACING IMAGE INFORMATION INTO A BUFFER LOCATION, WHEN DISPLAYED REPRESENTS A GREY SCALE OR COLOR SPECIFICATION WHEN SENT FOR DISPLAY. THE OUTPUT OF THESE LOCATIONS MAY ALSO BE USED FOR NON-VIDEO USE SUCH AS AUDIO, OR CONTROL OF OTHER DIGITAL DEVICES AT SLOWER RATES. IN THE 'STANDARD VERTICAL SPLIT' MODE, ADDRESS Ø (ZERO) APPEARS AT THE TOP LEFT CORNER OF THE DISPLAY FOR THE TOP BUFFER. ADDRESS 1 (ONE) APPEARS IMMEDIATELY TO THE RIGHT OF PIXEL ZERO, ON THE TOP LINE (LINE ZERO), ADDRESS 2 (TWO) TO THE RIGHT OF PIXEL 1 (ONE) AND SO ON, UP TO PIXEL ADDRESSED AT 127. PIXEL 127 IS THE RIGHTMOST ELEMENT ON THE TOP LINE. ADDRESS 128 APPEARS ONE LINE DOWN (LINE ONE), AT THE LEFT SIDE OF THE DISPLAY. PIXEL 129 IS ADJACENT ON THE RIGHT TO 128 AND 255 BECOMES THE LAST PICTURE ELEMENT ON LINE ONE. PIXEL 256 IS THE LEFTMOST ELEMENT ON LINE 2 ETC. THIS CONTINUES FOR THE TOP HALF OF THE DISPLAY UNTIL ADDRESS 8191, THE LAST ADDRESS IN THE TOP BUFFER, WHICH APPEARS AT THE RIGHTMOST SIDE OF LINE 63.

ADDRESS Ø (ZERO) OF THE BOTTOM BUFFER APPEARS AT THE LEFTMOST SIDE OF LINE 64, AND IS ADDRESSED IN A SIMILAR FASHION TO THE TOP BUFFER, WITH ADDRESS 8191 LOCATED AT THE BOTTOM RIGHT OF THE DISPLAY SCREEN.

FROM THE ABOVE DESCRIPTION AND FIGURE 3, CERTAIN ALGEBRAIC EQUATIONS MAY BE DERIVED.

HORIZONTAL MOVEMENT:

TO GET FROM ONE PIXEL TO THE PIXEL TO ITS IMMEDIATE RIGHT, WE ADD ONE TO THE ADDRESS. TO GET FROM THE CURRENT PIXEL TO THE PIXEL AT ITS IMMEDIATE LEFT, WE SUBTRACT ONE ADDRESS. AT THE RIGHTMOST PIXEL ON A LINE, THE ADDITION OF ONE CAUSES A 'WRAP-AROUND' TO THE LEFTMOST ELEMENT OF THE NEXT LINE DOWN. EXAMPLE: ADDITION OF 1 TO PIXEL 255 (2ND LINE RIGHTMOST PIXEL), YIELDS 256 THE LEFTMOST PIXEL OF LINE 2. WHEN AT THE LEFTMOST ELEMENT ON A LINE, SUBTRACTING ONE CAUSES AN UPWARDS 'WRAP-AROUND', TO THE RIGHTMOST ELEMENT OF THE LINE ABOVE.

A VARIABLE CALLED ''H' MAY BE INTRODUCED AS THE VALUE, TO BE ADDED OR SUBTRACTED TO YIELD THIS HORIZONTAL MOVEMENT. THE VARIABLE H IS SET TO ONE ADDRESS UNIT . . . H=1. ADDITION OF H TO THE CURRENT BUFFER ADDRESS, MOVES US ONE PIXEL TO THE RIGHT (AS DESCRIBED ABOVE), AND SUBTRACTING H MOVES US ONE PIXEL TO THE LEFT. SIMILARLY, ADDITION OF 3*H MOVES US THREE PIXEL TO THE RIGHT, AND ADDING -3*H MOVES US 3 PIXELS TO THE LEFT. EQUATIONS MAY BE WRITTEN FOR SPECIFYING ADDRESSING SCHEMES USING THE HORIZONTAL H IN THE EQUATIONS.

VERTICAL MOVEMENT:

TO GET FROM A PIXEL TO THE ONE IMMEDIATELY BELOW, WE ADD THE NUMBER 128 TO THE CURRENT PIXEL ADDRESS. TO GO TO THE PIXEL IMMEDIATELY ABOVE THE CURRENT ONE, WE SUBTRACT 128 FROM THE CURRENT PIXEL ADDRESS. TO GO TO THE PIXEL IMMEDIATELY ABOVE THE CURRENT ONE, WE SUBTRACT 128 FROM THE CURRENT PIXEL ADDRESS. WHEN SUBTRACTING 128 FROM A PIXEL ON THE TOPMOST LINE (LINE ZERO OF A BUFFER), WE CAUSE A VERTICAL 'WRAP-AROUND' TO THE BOTTOM-MOST LINE OF THAT BUFFER IN THE SAME 'COLUMN'. ADDITION OF 128 TO A PIXEL ADDRESS ON THE BOTTOM-MOST LINE OF A BUFFER CAUSES A VERTICAL WRAP-AROUND TO THE TOPMOST LINE OF THAT BUFFER. EXAMPLE: ADDING 128 TO ADDRESS 8190, BRINGS US TO ADDRESS 126, THE PIXEL 2ND FROM THE RIGHT ON LINE 0.

A VARIABLE NAMED 'V' MAY BE INTRODUCED, AS THE VALUE TO BE ADDED OR SUBTRACTED FOR VERTICAL POSITIONING. V IS SET EQUAL TO 128: V=128 ADDRESSES. ADDITION OF V CAUSES A POSITIONING TO THE LINE BELOW, AND SUBTRACTION OF V CAUSES POSITIONING TO THE LINE ABOVE THE CURRENT PIXEL (AS DESCRIBED ABOVE).

BY USING THESE VARIABLE H AND V, EQUATIONS MAY BE WRITTEN TO DETERMINE NEW POSITIONS FROM A CURRENT POSITION. TO MOVE 7 ELEMENTS RIGHT AND TWO ELEMENTS DOWN, WE CAN SET OUR ADDRESS = ADDRESS (OLD) + 7*H + '-2*V. IF CARE IS TAKEN TO EXAMINE THE WRAP-AROUND CONDITIONS (EITHER IN LOOP PARAMETERS OR ACTUAL TESTS), SIMPLE LINEAR EQUATIONS CAN SPECIFY POSITION. SINCE THE VERTICAL INCREMENT V IS A BINARY MULTIPLE, THE MULTIPLICATION MAY BE EASILY CALCULATED AS 7 SHIFT LEFT OPERATIONS, OR MULTIPLE ADDITIONS. FOR FIXED INCREMENTS ALONG THE HORIZONTAL AND VERTICAL, CONSTANTS MAY RESIDE IN THE 'EMIT' GROUP FOR ADDITION THROUGH THE ALU TO CALCULATE A NEW ADDRESS FROM THE CURRENT ONE.

CO-ORDINATE REPRESENTATION:

THE MEMORY BUFFERS MAY BE ADDRESSED, BY USING AN X-Y CARTESIAN CO-ORDINATE SYSTEM. IF WE SET THE DISPLAY ORIGIN AT THE TOP LEFT CORNER OF THE SCREEN, AN (X-Y) COORDINATE WOULD BE TRANSLATED TO BUFFER ADDRESS AS FOLLOWS:

1) FOR THE TOP BUFFER

(X,Y) = X*H+Y*V = X*1+Y*128 = X+128*Y = BUFFER ADDRESS

WITH X GOING FROM 0 TO 127, AND Y BETWEEN 0 AND 63.

2) FOR THE TOP BUFFER

(X,Y)=X*H+(Y-64)*V = X*1+128*(Y-64)

X FROM 0 TO 127, Y FROM 64 TO 127.

THE Y VALUE DETERMINES IF THE PIXEL IS LOCATED IN THE TOP OR BOTTOM BUFFER (EQUATION 1). IF Y IS LESS THAN 64, THE PIXEL IS IN THE TOP BUFFER, BUT WHEN GREATER OR EQUAL TO 64, IT APPEARS IN THE BOTTOM OR LOWER BUFFER (EQUATION 2).

IF X AND Y ARE HELD BETWEEN ZERO AND 127, THE ABOVE TEST AND EQUATIONS PLACE THE X-Y CO-ORDINATE INTO THE APPROPRIATE BUFFER POSITION.

HIGHER DENSITY DISPLAY:

WHEN DISPLAYING THE BUFFERS IN A HIGHER DENSITY MODE (MORE PIXELS PER LINE, AND 256 OR 512 LINES PER FIELD), SIMILAR EQUATIONS MY BE APPLIED, WITH MINOR CHANGES TO THIS ADDRESSING, BY CHANGING H AND V AND CHANGING THE TEST FOR WHICH BUFFER THE PIXEL IS LOCATED IN.

LIMITATIONS OF THE 'STANDARD VERTICAL SPLIT' MODE:

THIS MODE OF OPERATION IS EXTREMELY USEFUL WHEN SCREEN OPERATIONS CAN BE SEPARATED INTO TOP AND BOTTOM HALVES OF THE SCREEN, BUT IS INAPPROPRIATE WHEN DOING OPERATIONS, EXCHANGING PIXELS FROM THE TOP AND BOTTOM OF THE SCREEN. THIS IS A LIMITATION ONLY WHEN REAL TIME PROCESSING IS DONE SIMULTANEOUSLY TO ACQUISITION OF AN IMAGE. IF THE NECESSITY OF REAL TIME MUST HOLD, PROCESSING IN THE BLANKING INTERVAL MAY BE DONE, OR A DIFFERENT TIMING ALLOCATION FROM THE VERTICAL SPLIT MAY BE USED (SAY HORIZONTAL SPLIT). COMPLETELY RANDOM ADDRESSING OF A BUFFER IN WHICH AN IMAGE IS BEING ACQUIRED, WILL HAVE TO USE THE BLANKING INTERVALS, TO AVOID CONFLICT WITH THE WRITE OPERATION (THE BUFFER WRITE CYCLES) WHEN PIXEL 'COLLISION' OCCURS, OR A COPY OF THE BUFFER MAY BE MADE AND THEN PROCESSED WITHOUT REGARD FOR THE DISPLAY TIMING.

DISCNAME: 0
FILENAME: PXPROC
UPDATED: 28-NOV-79

PIXEL PROCESSOR/CONTROLLER

THE HIGH SPEED VIDEO PIXEL PROCESSOR CO-ORDINATES FAST TRANSFERS TO AND FROM THE EIGHT IMAGE BUFFERS IN A REAL TIME PROCESSING MODE, OR OTHER CONTROL PROCESSES WHEN NOT ENGAGED IN BUFFER MANIPULATION.

CONTROL STORE SEQUENCER

THE PIXEL PROCESSOR IS IMPLEMENTED AS A MICRO-PROGRAMMED PROCESSOR WITH A CYCLE TIME OF 200 NS. (A 5 MEGAHERTZ CLOCK). IT CONTAINS A WRITABLE CONTROL STORE, 256 WORDS BY 80 BITS WIDE. THE CONTROL STORE MAY BE POTENTIALLY EXPANDED UP TO 4096 WORDS, WHICH IS USEFUL, WHEN 'PROMMED' VERSIONS OF MICRO-CODE ARE DEVELOPED. THE ARITHMETIC/LOGIC SECTION HAS A 16 BIT WIDE DATA PATH, WITH THREE OPERAND FIELDS: TWO INPUT SOURCES, AND ONE OUTPUT. THE ARITHMETIC/LOGIC SECTION CONTAINS A 16 WORD REGISTER STACK AND A 'Q REGISTER' FOR TEMPORARY STORAGE OF IMAGING PARAMETERS.

THE PIXEL PROCESSOR IS COMPOSED OF THE FOLLOWING COMPONENT BLOCKS:

1) CONTROL UNIT

A) CONTROL STORE SEQUENCER
B) WRITABLE CONTROL STORE (PIPELINE REGISTER)
C) TEST CONDITION SELECTOR

2) ARITHMENTIC/LOGIC UNIT

A) A 16 BIT ALU
B) AN INTERNAL 16 WORD BY 16 BIT REGISTER STACK AND A Q REGISTER
C) INPUT SELECTORS FOR 'A' AND 'B' INPUT TO THE ALU
D) AN OUTPUT SELECTOR FOR ROUTING TO 'EXTERNAL' REGISTERS
E) A SPECIAL BUFFER 'PRE-SELECTOR' TO ROUTE BUFFERS TO ALU INPUT
F) A POST-FORMAT SELECTOR TO RE-ROUTE THE ALU OUTPUT (BY 4 BIT NIBBLES) TO EXTERNAL REGISTERS

3) MEMORY ADDRESSING UNIT

4) BUS INTERFACE LOGIC

5) TIMING AND CONTROL LOGIC

C- AND D- ADDRESS UNITS

TO GENERATE ADDRESSES FOR BUFFER MANIPULATION, TWO INDEPENDENT ADDRESS FORMATION UNITS ARE PRESENT, EACH GENERATING A SIXTEEN BIT ADDRESS ON SEPARATED ADDRESS BUSES. SIXTEEN BITS ALLOW FOR ADDRESSING UP TO 64K WORDS FOR EACH BUFFER, CORRESPONDING TO A 256 BY 256 BY N BIT DEEP BUFFER. THIS ENABLES FORESEEABLE EXPANSION OF THE BUFFER SPACE FOR HIGHER RESOLUTION IMAGES.

AS THIS PROCESSOR IS PART OF A DEVELOPMENT SYSTEM, CERTAIN PROTOTYPING PROVISIONS ARE INCLUDED:

A) RUN/HALT OF PROCESSOR CLOCK
B) INDEPENDENT SINGLE STEPPING OF PIPELINE CLOCK AND ALU/SEQUENCER CLOCK
C) LOADING CONTROL STORE
D) 'MEMORY TRAP' - HALTS THE PROCESSOR WHEN IT 'FALLS OFF' THE EDGE OF THE CONTROL STORE, WHEN ATTEMPTING TO ACCESS NON-EXISTANT CONTROL STORE LOCATIONS.
E) EXAMINATION AND CHANGE OF ALL INTERNAL AND EXTERNAL ALU REGISTERS.
F) COMPLETE CONTROL OF PIPELINE REGISTER TO 'FORCE' INSTRUCTIONS IN SINGLE STEP MODE (READ AND WRITE).

THESE HARDWARE PROVISIONS ALONG WITH AN INTERACTIVE MICRO-ASSEMBLER (ON THE LSI-11) ASSIST IN MICRO-PROGRAM DEBUGGING PROGRAM DEVELOPMENT.

DISCNAME: 0
FILENAME: BUFFER
UPDATED: 25-NOV-79

BUFFER DESCRIPTION

THE IMAGE BUFFERS ARE PHYSICALLY ORGANIZED AS MEMORY PLANES OF 8K WORDS (K=1024) BY 16 BIT DEEP. EACH OF THESE PLANES MAY BE FURTHER SUBDIVIDED OR SEGMENTED AS 8K BY 4 BIT GROUPINGS. FOUR BUSES ENTER EACH MEMORY PLANE TO ALLOW INDEPENDENT ACCESS TO THE SEGMENTS BY DIFFERENT BUSES. ACCESS TO THE ENTIRE MEMORY PLANE IS ACCOMPLISHED THROUGH ACCESSING ALL SEGMENTS SIMULTANEOUSLY THROUGH ONE BUS.

A MASTER PRIORITY REGISTER DETERMINES THE USAGE HIERARCHY FOR CONFLICTS IN BUFFER ACCESS. THIS PRIORITY REGISTER IS SET BY THE CONTROLLING CPU AND ONCE SET, IT DETERMINES THE CURRENT HIERARCHY. CONTROL OF A MEMORY SEGMENT IS GIVEN TO THE DEVICE WITH THE GREATEST PRIORITY LEVEL AT THE END OF THE CURRENT MEMORY CYCLE. A LATENCY TIME OF ONE MEMORY CYCLE IS PRESENT FROM ISSUING A REQUEST TILL IT IS GRANTED, IF THE MEMORY SEGMENT IS IN USE.

EACH DEVICE HAS ITS OWN REQUEST/GRANT REGISTER. UPON REQUESTING USE OF A MEMORY SEGMENT, THE GRANT REGISTER INDICATES WHEATHER THE REQUEST IS GRANTED OR NOT. EACH DEVICE HAS ACCESS TO ONE ADDRESS IN ALL FOUR SEGMENTS AT A TIME, UNLESS THE DEVICE OCCUPIES TWO INDEPENDENT BUSES.

ONCE CONTROL OF A MEMORY SEGMENT IS ATTAINED, TRANSFER RATES MAY BE EXECUTED AT THE CYCLE TIME OF THE MEMORY. THE ACCESS TIMES AND CYCLE TIMES ARE IDENTICAL AND FIXED AT 200 NANOSECOND TIME INTERVAL. THE BUFFER IS 'STATIC' IN FORMAT AND NO REFRESHING OR SPECIAL TIMING RESTRICTIONS NEED BE FOLLOWED BY THE REQUESTING DEVICE FOR READING OR WRITING TO THE MEMORY SEGMENT - THIS TIMING IS INTERNALLY DECODED.

A SPECIAL CPU 'SOFT' REGISTER IS AVAILABLE FOR SELECTION OF MEMORY SEGMENTS BY A CENTRAL SOURCE (THE CPU). THIS REGISTER IS IDENTIFIED AS A 'SOFT REQUEST REGISTER' AND ALLOWS CONNECTION TO TIMING LOGIC WITHOUT THE NEED TO RECOGNIZE THE REQUEST/GRANT SEQUENCE.

A SECOND 'SOFT READ-WRITE REGISTER' IS CONCURRENTLY USED TO DETERMMINE THE MODE OF THE SOFT SELECTED MEMORY SEGMENT.

THE BUFFER INPUTS

THE BUFFER HAS FOUR PRINCIPLE PROCESSING UNITS ATTACHED TO ITS OPERATION:

1) THE X-Y DISPLAY LOGIC:
THIS LOGIC DETERMINES THE ADDRESSING SCHEME TO MAP THE MEMORY ADDRESSES INTO HORIZONTAL AND VERTICAL SCREEN COORDINATES. THIS IS ACCOMPLISHED THROUGH A COUNTER CHAIN WHICH DIVIDES A HIGH FREQUENCY CLOCK, TO DETERMINE SCREEN POSITION. A DISPLACEMENT IN THIS ADDRESSING SCHEME RESULTS IN A DISPLACEMENT OF THE PICTURE INFORMATION TO SCREEN POSITION.

2) THE CENTRAL PROCESSING UNIT
THE CPU ACCESSES A BUFFER AS A MEMORY ARRAY. THE CHANGE OF INFORMATION CONTENT MUST BE TIME-LOCKED TO THE X-Y DISPLAY LOGIC, TO AVOID BREAK-UP OF THE DISPLAYED IMAGE.

3) AN EXTERNALLY SUPPLIED DIGITAL IMAGE SOURCE:
AN INPUT IS MAINTAINED TO ALLOW ACQUISITION OF A REAL TIME IMAGE SIGNAL, TIMED TO THE X-Y COORDINATES. THIS ACCOMPLISHES 'FRAME GRABBING' OF A VIDEO IMAGE IN 1/60 OF A SECOND.

4) A HIGH SPEED PIXEL PROCESSOR/CONTROLLER:
THIS DEVICE IS A MICROPROGRAMMED MACHINE WITH A CYCLE TIME OF 200 NANOSECONDS. ITS CURRENT ROLES INCLUDE: POSITION TRANSFORMATIONS ON THE BUFFER CONTENTS, VECTOR TO RASTER CONVERSION, TRANSLATION OF GRAY SCALE AND COLOR RENDITION, AND INFORMATION TRANSFER BETWEEN IMAGE SEGMENTS AND PLANES.

READ CYCLE:

THE READ CYCLE CONSISTS OF THE FOLLOWING SUB-CYCLES, INTERNALLY GENERATED BY THE BUFFER TIMING LOGIC:

1) AT THE BEGINNING OF THE CYCLE, THE PRIORITY REQUEST LOGIC 'SWITCHES' THE BUFFER TO THE CURRENTLY ACTIVE BUS, AS DETERMINED IN THE PREVIOUS CYCLE'S PRIORITY REQUEST. THE 'SWITCH' INVOLVES CHANGING THE SIGNALS THAT CONTROL THE DATA, ADDRESS AND CONTROL MULTIPLEXERS.

2) INFORMATION ON THE DATA, ADDRESS AND CONTROL LINES OF THE SELECTED BUS, ROUTE THROUGH THE BUS SELECTORS (MULTIPLEXERS) TO EDGE TRIGGERED LATCHES. THESE LATCHES ARE THEN CLOCKED, HOLDING THE CURRENT ADDRESS DATA AND CONTROL INFORMATION, FOR THE DURATION OF THE MEMORY CYCLE. THIS LATCHING OF INFORMATION FACILITATES CORRECT OPERATION OF THE BUFFER WITH LESS THAN OPTIMUM INPUTS (THE LATCH HAS AN INPUT APERTURE OF 8 NANOSECONDS), AND ALSO FREES EXTERNAL DEVICES FROM GENERATING THE MEMORY TIMING.

3) THE LATCHED OUTPUTS ARE PRESENTED TO THE 8K WORD BY 4 BIT MEMORY BUFFER, AND INITIATE THE READ CYCLE. THE MEMORY THEN ACCESSES THE ADDRESSED LOCATION AFTER A FINITE TIME (THE 'READ ACCESS TIME' FROM ADDRESS TILL DATA OUTPUT, OF 120 NANOSECONDS). THIS OUTPUT IS THEN FED TO THE OUTPUT LATCH.
4) THE OUTPUT LATCH IS STROBED AND MARKS THE END OF THE MEMORY CYCLE. THE OUTPUT LATCH NOW CONTAINS THE ADDRESSED DATA.

WRITE CYCLE:

THE WRITE CYCLE BEGINS IDENTICALLY TO THE READ CYCLE:

1) THE CORRECT BUS IS SWITCHED IN BY THE PRIORITY LOGIC AT THE BEGINNING OF THE CYCLE.
2) THE DATA IS ROUTED THROUGH THE SELECTORS AND CLOCKED INTO THE STORAGE LATCHES.
3) AT THIS STEP THE LATCHED READ/WRITE LINE DETERMINES IF A WRITE CYCLE WILL BE PERFORMED. IF THIS LINE IS LOW, SIGNIFYING A WRITE REQUEST, A WRITE CYCLE BEGINS. THE LOOP-AROUND LOGIC IS SWITCHED TO ACCEPT THE CURRENTLY LATCHED INPUT DATA AND PASS IT ALONG TO THE OUTPUT LATCH. WHILE THIS IS GOING ON, THE 'WRITE PULSE GENERATION LOGIC' IS ENABLED BY THE LATCHED READ/WRITE CONTROL LINE. THE CORRECT TIMING PULSE IS GATED TO THE READ/WRITE LINE ON THE BUFFER MEMORY CHIPS. THIS PULSE IS SLIGHTLY SHORTER VERSION OF READ CYCLE TIMING (GREATER THAN 60 NANOSECONDS). AT THE END OF THIS PULSE, THE WRITE OPERATION IS COMPLETED. THE MEMORY CHIPS REMAIN ENABLED FOR THE DURATION OF THE CYCLE.
4) THE DATA THAT PASSED THROUGH THE 'LOOP-AROUND' LOGIC IS NOW STROBED INTO THE OUTPUT LATCH. THE WRITTEN DATA IS PRESENTED TO THE OUTPUT, MARKING THE END OF THE CYCLE.

TIMING FOR THE BUFFERS IS GENERATED ON CARD, FOR ALL FOUR BUFFERS. EACH BUFFER OPERATES ON A MEMORY CYCLE OF 200 NANOSECOND DURATION. ONCE A DEVICE IS GRANTED USAGE OF THE BUFFER, THE DEVICE REQUESTS A READ OR WRITE CYCLE. THIS REQUEST IS PLACED ON THE READ/WRITE CONTROL LINE.

SIMULTANEOUS TO THE EXECUTION OF A READ OR WRITE CYCLE, THE PRIORITY REQUEST LOGIC DETERMINES BUS CONTROL FOR THE NEXT CYCLE. MEMORY CYCLES ARE CLOCKED OPERATIONS, DERIVED FROM THE X1 CLOCK RATE (200 NANOSECONDS, 5 MEGAHERTZ). A SHORT GRACE PERIOD IS INCLUDED TO COMPENSATE FOR PROPAGATION DELAYS, AND ALSO CABLE DELAY FROM THE DRIVING DEVICE TO THE BUFFER.

LSI-11
REGISTERS

DISCNAME: X
FILENAME: REGS.DOC
UPDATED: 24-NOV-80

L S I - 1 1 R E G I S T E R A S S I G N M E N T

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ALL REGISTERS ARE BYTE ADDRESSABLE EXCEPT MICRO-REGISTERS 164140-164166 WHICH ARE "WORD ORIENTED" REGISTERS. BYTE ADDRESSING OF THE MICRO-REGISTERS MAY CAUSE ERRONEOUS RESULTS. UNUSED BITS SHOULD NOT BE ASSUMED TO READ AS ONE OR ZERO, AND SHOULD THEREFORE BE 'MASKED OFF' IN A REGISTER (OR MAIN MEMORY) BEFORE PROGRAM USAGE.

164000-164076 IS THE PHANTOM REGION; REGISTER-WRITE ONLY, BUT MAY BE READ THROUGH THE PHANTOM PARODY OF THE REGISTERS' DATA.

BUFFER OUTPUT DISPLAY REGISTERS:	:OUTP.3 :OUTP.2 :OUTP.1 :OUTP.0 :1	
	:OUTP.3 :OUTP.2 :OUTP.1 :OUTP.0 :164002	
	:OUTP.3 :OUTP.2 :OUTP.1 :OUTP.0 :164004	
	:OUTP.3 :OUTP.2 :OUTP.1 :OUTP.0 :164006	
BITS 0-15	:LSI-11 COMMUNICATE OUT :164010	
	: FREE :164012	
A BUS REQ. REG. BITS 0-7:	:LSI-11 REQUEST :164014	
L=UNREQ., H=REQ.		
LINE MATCH, BITS 0-11	:LINE MATCH REGISTER :164016	
8 ADDRESS UNITS, SCREEN OFFSET REGS BITS 0-11	:X0 OFFSET :1	
	:Y0 OFFSET :164022	
	:X1 OFFSET :164024	
	:Y1 OFFSET :164026	
FOR FUTURE EXPANSION	:X2 OFFSET :164030	
	:Y2 OFFSET :164032	
	:X3 OFFSET :164034	
	:Y3 OFFSET :164036	

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B ADDRESS UNIT CONTROL :ADDRESS UNIT 1 :ADDRESS UNIT 0 :164040
REGISTERS, BITS 0-7,8-15:::::::::::::::::::::::::::::::::
FOR FUTURE EXPANSION....:ADDRESS UNIT 3 <-  :ADDRESS UNIT 2 :16
                         :::::::::::::::::::::::::::::::::
B BUS BUFFER MODE        :BUF 3  :BUF 2  :BUF 1  :BUF 0  :164044
REGISTERS                :::::::::::::::::::::::::::::::::
BITS 0-3,4-7,8-11,12-15 <-  :BUF 7  :BUF 6  :BUF 5  :BUF 4  :16
                         :::::::::::::::::::::::::::::::::
B BUS REQ. BITS 0-7      :             :QUAD 0          :164050
1=UNREQ., L=REQ.         :::::::::::::::::::::::::::::::::
                         :             :QUAD 1          :164052
                         :::::::::::::::::::::::::::::::::
                         :             :QUAD 2          :164054
                         :::::::::::::::::::::::::::::::::
                         :             :QUAD 3          :164056
                         :::::::::::::::::::::::::::::::::
BUFFER PRIORITY/         :SOFT REQUEST 0 :BUF 0 PRIORITY :164060
SOFT REQUEST             :::::::::::::::::::::::::::::::::
BITS 0-7,8-15            :SOFT REQUEST 1 :BUF 1 PRIORITY :164062
                         :::::::::::::::::::::::::::::::::
                         :SOFT REQUEST 2 :BUF 2 PRIORITY :164064
                         :::::::::::::::::::::::::::::::::
                         :SOFT REQUEST 3 :BUF 3 PRIORITY :164066
                         :::::::::::::::::::::::::::::::::
                         :SOFT REQUEST 4 :BUF 4 PRIORITY :164070
                         :::::::::::::::::::::::::::::::::
                         :SOFT REQUEST 5 :BUF 5 PRIORITY :164072
                         :::::::::::::::::::::::::::::::::
                         :SOFT REQUEST 6 :BUF 6 PRIORITY :164074
                         :::::::::::::::::::::::::::::::::
                         :SOFT REQUEST 7 :BUF 7 PRIORITY :164076
                         :::::::::::::::::::::::::::::::::
A BUS BUFFER GRANT       :             :BUFFER GRANT    :164100
BITS 0-7                 :::::::::::::::::::::::::::::::::
READ BACK FOR FPLA(PROM):PRIORITY  CONTROL  READ        :164102
BITS 0-15                :::::::::::::::::::::::::::::::::
BITS 0-7                 :             :PRIOR CYCLE EN  :164104
                         :::::::::::::::::::::::::::::::::
BITS 0-11                :       :READ LINE COUNT REG.  :164106
                         :::::::::::::::::::::::::::::::::
BITS 0-15                :LSI-11 COMMUNICATION IN       :164110
                         :::::::::::::::::::::::::::::::::
BUFFER READBACK BITS 0-3 :QUAD & BUFFER READ BACK CONTROL:164112
QUAD CONTROL BITS 4-7    :::::::::::::::::::::::::::::::::
'PAGE' EXTENDED ADDRESS  :             <-  :PAGE EXT. ADDR.:16
BITS 0-7                 :::::::::::::::::::::::::::::::::  164114
                         :             FREE             :164116
TITLER CONTROL BITS 0-7  :::::::::::::::::::::::::::::::::
KEY SELECT BITS 8-11     :       :SEL/POL:TITLER CONTROL :164120
KEY POLARITY BIT 11      :::::::::::::::::::::::::::::::::
                         :BLINK  :V.SPACE:H.SIZE :V.SIZE :164122
                         :::::::::::::::::::::::::::::::::
                         :WINDOW X1 (BEG):WINDOW Y1      :164124
                         :::::::::::::::::::::::::::::::::
                         :WINDOW X2      :WINDOW Y2 (END):164126
                         :::::::::::::::::::::::::::::::::
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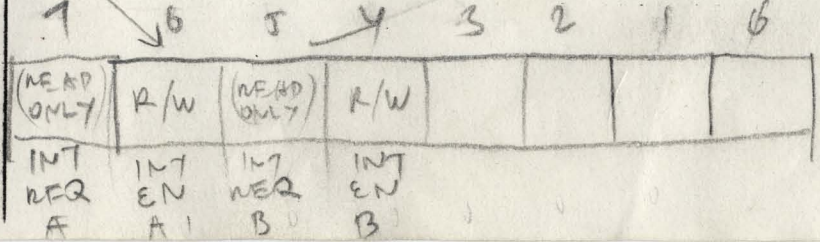
A-MATTE, BITS 0-11      :        :A-MATTE                    :164130
                        :::::::::::::::::::::::::::::::::::::
B-MATTE, BITS 0-11      :        :B-MATTE                    :164132
                        :::::::::::::::::::::::::::::::::::::
D TO A, BITS 0-15       :D TO A CONTROL                      :164134
                        :::::::::::::::::::::::::::::::::::::
BITS 0-15               :D TO A MAP ADDRESS SELECT           :164136
                        :::::::::::::::::::::::::::::::::::::
BITS 0-15               :MICRO CONTROL/STATUS                :164140
                        :::::::::::::::::::::::::::::::::::::
BITS 0-11               :        :MICRO ADDRESS              :164142
                        :::::::::::::::::::::::::::::::::::::
PIPELINE REGISTERS      :GROUP 0 = PIPE 0-15                 :164144
BIT  0 IS PIPE 0        :::::::::::::::::::::::::::::::::::::
BIT 15 IS PIPE 15       :GROUP 1 = PIPE 16-31                :164146
BIT  0 IS PIPE 16       :::::::::::::::::::::::::::::::::::::
BIT 15 IS PIPE 31       :GROUP 2 = PIPE 32-47                :164150
ECT...                  :::::::::::::::::::::::::::::::::::::
                        :GROUP 3 = PIPE 48-63                :164152
                        :::::::::::::::::::::::::::::::::::::
                        :GROUP 4 = PIPE 64-79                :164154
                        :::::::::::::::::::::::::::::::::::::
FOR FUTURE EXPANSION:   :GROUP 5 = PIPE 80-95                :164156
                        :::::::::::::::::::::::::::::::::::::
                        :SEQUENCER STATUS                    :164160
                        :::::::::::::::::::::::::::::::::::::
                        :        :DIRECT INPUT READBACK      :164162
                        :::::::::::::::::::::::::::::::::::::
                        :                FREE                :164164
                        :::::::::::::::::::::::::::::::::::::
BITS 0-15               :ALU OUTPUT READ BACK                :164166
                        :::::::::::::::::::::::::::::::::::::
                        :                FREE                :164170
                        :::::::::::::::::::::::::::::::::::::
                        :                FREE                :164172
                        :::::::::::::::::::::::::::::::::::::
OPTIONAL PLUG IN        :TEST PORT                           :164174
                        :::::::::::::::::::::::::::::::::::::
                        :LSI-11 STATUS/CONTROL               :164176
                        :::::::::::::::::::::::::::::::::::::
```



1 = VECTOR = 200

NOT 170

BOUT
BAD
B-MODE
BREQ
LSI READBACK
SRE
PSET

DISCNAME: X
FILENAME: BBUS.DOC
UPDATED: 24-NOV-80

B-BUS ADDRESS AND CONTROL REGISTERS

THE ADDRESSING UNITS ACCESS THE IMAGE BUFFERS THROUGH REQUEST/GRANT SIGNALS, TIMED TO THE HORIZONTAL AND VERTICAL VIDEO RATES. IT UTILIZES A QUADRANT METHOD OF ACCESS, SPLITTING THE SCREEN INTO FOUR REGIONS:

THE TOP LEFT QUADRANT - QUADRANT 0
THE TOP RIGHT QUADRANT - QUADRANT 1
THE BOTTOM LEFT QUADRANT - QUADRANT 2
THE BOTTOM RIGHT QUADRANT - QUADRANT 3

THE ADDRESSING UNITS READ OR WRITE TO EACH OF THESE QUADRANTS INDEPENDENTLY, ALLOWING COMBINATIONS OF PRIORITIZED ACCESS TO THE BUFFERS. THE QUADRANT RELATED REGISTERS ARE:

1) THE BUFFER OUTPUT DISPLAY REGS (BOUT) 164000-164006
2) THE ADDRESS MODE REGISTERS (BAD) 164040-164042
3) B-BUS BUFFER MODE REGISTERS (BMODE) 164044-164046
4) THE B-BUS REQUEST REGISTERS (BREQ) 164050-164056
5) QUAD CONTROL/LSI-11 READBACK REGISTER 164112
6) Priority/Soft Request Reg (PSET) X060-X076

OUT 0 = RED
OUT 1 = GNE
OUT 2 = BLU
OUT X = X

} THROUGH TIMER

X DIRECTLY FROM OUTPUT SELECTOR

1) BUFFER OUTPUT DISPLAY REGISTERS:

THESE REGISTERS, ORGANIZED BY QUADRANTS (0 TO 3), DETERMINE WHICH OF THE EIGHT BUFFERS (OR BLACK) WILL BE DISPLAYED IN EACH OF THE FOUR QUADRANTS OF THE SCREEN. THE FOUR OUTPUT CHANNELS ARE ASSIGNED BY PLACING THE BIT PATTERN (SEE TABLE BELOW) INTO THE REGISTERS' NIBBLE POSITION.

X B G R

OUTPUT #3	OUTPUT #2	OUTPUT #1	OUTPUT #0	
15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	QUADRANT 0
BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	QUADRANT 1
BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	QUADRANT 2
BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	BK S2 S1 S0	QUADRANT 3

QUADRANT 0 IS ADDRESS 164000 QUADRANT 1 IS ADDRESS 164002
QUADRANT 2 IS ADDRESS 164004 QUADRANT 3 IS ADDRESS 164006

TABLE:

BK	S2	S1	S0	OUTPUT
0	0	0	0	BUFFER 0
0	0	0	1	BUFFER 1
0	0	1	0	BUFFER 2
0	0	1	1	BUFFER 3
0	1	0	0	BUFFER 4
0	1	0	1	BUFFER 5
0	1	1	0	BUFFER 6
0	1	1	1	BUFFER 7
1	X	X	X	'BLACK' (ALL ZEROS)

WHERE: 0 = LOW 1 = HIGH AND X = DON'T CARE

2) ADDRESS MODE REGISTERS:

THE ADDRESS MODE REGISTER CONTROLS THE TWO ADDRESS UNITS OPERATION. IT ASSIGNS RESOLUTION, DIRECTION OF ADDRESSING (UP/DOWN, LEFT/RIGHT), AND THE RE-MAPPING OF THE ADDRESS BY THE ADDRESS MAP UNIT. THE LOWER BYTE (BAD 0) SERVICES BUFFERS 0-3, AND THE UPPER BYTE (BAD 1) BUFFERS 4-7.

REGISTER: 164040

!15(7)	!14(6)	!13(5)	!12(4)	!11(3)	!10(2)	!9(1)	!8(0) !
X RESOLUTION		Y RESOLUTION		X MAP	L/R DIREC	Y MAP	U/D DIREC

BITS 0 AND 2 (8 AND 10) - SCAN CONVERTING BITS(L):
WHEN LOW, THESE BITS REVERSE THE OUTPUT DISPLAY RIGHT FOR LEFT (BIT2/10), AND UPSIDE DOWN (BIT 0/8).

BITS 1 AND 3 (9 AND 11) - MAPPING BITS(H):
WHEN SET, THEY PLACE THE BUFFER INTO A MAPPED ADDRESS MODE. THE BUFFER DISPLAY ADDRESS (PIXEL LOCATION) IS DECIDED BY THE MEMORY MAP DRIVEN BY THE X AND Y GENERATORS. THESE MAPS ARE LOADED BY THE VIDEO PROCESSOR AND GIVE ACCESS TO QUICK COMPRESSION AND EXPANSION OF THE X AND Y TIME AXIS, BY CHANGING THE VALUE OF THE MAP.

BITS 4 AND 5 (12 AND 13) ARE THE Y RESOLUTION

BITS 6 AND 7 (14 AND 15) ARE THE X RESOLUTION

BIT5(7)	BIT4(6)	
0	0	NORMAL
0	1	HIGH
1	0	LOW
1	1	AUXILIARY

X-Y ADDRESS MAPS

SOME METHODS TO GENERATE ADDRESSES ARE:
A MAPPING MEMORY OF 256 WORDS BY 8 BITS IS PLACED ON THE OUTPUTS OF THE X/Y ADDRESS TIMING (ONE MAPPING MEMORY ON THE HORIZONTAL AND ONE ON THE VERTICAL TIMING). THESE MAPPING MEMORIES ARE LOADED WITH A FUNCTION WHICH TRANSLATE THE SEQUENTIAL X OR Y INTO A DIFFERENT ADDRESSING SCHEME. THE MAPPING MEMORIES ARE WRITTEN TO DURING THE INACTIVE SCAN (BLANKING, OR WHEN THE BUFFERS ARE NOT IN USE) AND MAP THE FUNCTION USED DURING THE ACTIVE SCAN. A DELAY OF THE X/Y ADDRESSING THROUGH THE MAPPING MEMORY MAY BE COMPENSATED BY SHIFTING THE X/Y ADDRESSING FORWARD AN EQUAL TIME DELAY. MAPPING MEMORIES PERMIT SOFTWARE SPECIFICATION, THE ALGORITHMS FOR COMPRESSION OR EXPANSION OF IMAGE WITHIN OUR TIME GRID. THESE MEMORIES COULD BE LOADED FROM THE LSI-11 DURING VERTICAL BLANKING OR BY THE VIDEO PROCESSOR. THESE MAPPING MEMORIES ARE ESSENTIALLY PROGRAMMABLE FUNCTION GENERATORS, TIMED TO THE X AND Y SIGNALS. THEY ARE LOADED BY THE PIXEL PROCESSOR THROUGH THE C-BUS.

GRAB WHEN φ GOES HI

3) B-BUS BUFFER MODE REGISTERS:

THE B-BUS CONTROL REGISTERS (164044 AND 164046) DETERMINE THE MODE OF A BUFFER WHEN THE REQUEST HAS BEEN GRANTED OR DURING A SOFT REQUEST. FOUR BITS ARE ASSIGNED TO EACH BUFFER TO DECIDE THE MODE:

REGISTER 164044: BUFFER 0-3
REGISTER 164046: BUFFER 4-7

BUFFER 3 (7)				BUFFER 2 (6)				BUFFER 1 (5)				BUFFER 0 (4)			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S3	S2	S1	S0	S3	S2	S1	S0	S3	S2	S1	S0	S3	S2	S1	S0

TABLE:

S3	S2	S1	S0	
0	X	X	0	NORMAL WRITE BUFFER
0	X	X	1	NORMAL READ BUFFER
1	X	X	0	TEST MODE

WHERE: 0 = LOW 1 = HIGH AND X = DON'T CARE

BITS 0 - 4 - 8 - 12 - READ/WRITE(L):
SETS THE MODE OF THE BUFFER DURING THE ACTIVE SCREEN, ENABLED BY THE REQUEST REGISTER. WHEN THE REQUEST IS ACTIVE, THE BUFFER IS PLACED IN A READ OR WRITE STATE DEPENDING ON THE STATE OF THIS BIT. THE WRITE OPERATION OCCURS ONLY DURING THE ACTIVE SCREEN.

BITS 1,2 - 5,6 - 9,10 - 13,14 - UNUSED

BITS 3 - 7 - 11 - 15 - TEST MODE(H)/WRITE-READ PIXEL(L):

BIT 3(L) - NORMAL MODE:
WHEN LOW, THIS BIT OPERATES IN CONJUNCTION WITH THE LOWER BITS (BITS 0 AND 1) TO ACTIVATE A FRAME GRABBING SIMILAR TO A READ-VERIFY-WRITE OPERATION. DATA IS WRITTEN IN FOR ONE PIXEL, THEN READ OUT IN THE NEXT ADJACENT PIXEL TO THE RIGHT. THIS OCCURS DURING ANY QUADRANT THAT HAS BEEN REQUESTED AND GRANTED, YIELDING A SIDE BY SIDE PIXEL TEST.

4) B-BUS REQUEST REGISTERS:

REQUESTS BY THE ADDRESSING UNIT TO THE BUFFERS ARE PLACED ON THE B BUS BY TIMING LOGIC, DRIVEN BY THESE REGISTERS. EACH BUFFER IS ASSIGNED FOUR QUADRANTS WHICH CORRESPOND TO THE FOUR CORNERS OF THE SCREEN. THESE REGISTERS ALLOCATE WHICH PORTION OF THE SCREEN WILL BE USED BY THE BUFFER, AND SHOULD BE SET UP ON A FIELD BY FIELD BASIS.

THE REGISTERS ARE FORMATTED:

BITS:	7	6	5	4	3	2	1	0	
REGISTER164050	R	R	R	R	R	R	R	R	QUADRANT 0
REGISTER164052	R	R	R	R	R	R	R	R	QUADRANT 1
REGISTER164054	R	R	R	R	R	R	R	R	QUADRANT 2
REGISTER164056	R	R	R	R	R	R	R	R	QUADRANT 3
BUFFERS:	7	6	5	4	3	2	1	0	

WHERE: R = 0 MEANS THE BUFFER IS ~~INACTIVE~~ IN THAT QUADRANT
R = 1 MEANS THE BUFFER IS ACTIVE IN THAT QUADRANT
...THE BUFFER IS REQUESTED WHEN 'R' IS SET TO A LOW

BITS 8 TO 15 - UNUSED

PUT 0(L) INTO THE REQUESTED QUADRANT

5) QUADRANT CONTROL REGISTER/LSI-11 BUFFER READBACK

THIS REGISTER HAS A DUAL FUNCTION. THE LOWEST FOUR BITS SELECT WHICH BUFFER IS READ BACK IN THE 1 K ADDRESS SPACE, BY THE LSI-11. THE OTHER BITS (4-7) CONTROL THE B-BUS QUADRANT LOGIC. THESE TWO FUNCTIONS ARE ASSIGNED FOUR BITS A PIECE, AND ARE ALIGNED IN THE REGISTER AS SHOWN BELOW:

REGISTER 164112

7	6	5	4	3	2	1	0
QC1	QC0	S1	S0	B3/ B7(H)	B2/ B6(H)	B1/ B5(H)	B0/ B4(H)
QUADRANT CONTROL				LSI-11 BUFFER READBACK			

BITS 0-3 ARE USED WHEN READING BACK THE CONTENTS OF THE BUFFER. THEY SELECT WHICH BUFFER IS READ IN THE FOUR BIT GROUPS OF THE 1K ADDRESS SPACE (LOCATIONS 160000-163776). A ZERO IN THE BIT SELECTS THE 'LOWER NUMBER'(0-3) BUFFER TO BE READ BACK IN THE FOUR BITS, AND A ONE SELECTS THE 'HIGHER NUMBER'(4-7) BUFFER OF THE PAIR.

BIT 0 - BUFFER 0(L)/BUFFER 4(H)
A ZERO SELECTS BUFFER 0 A ONE SELECTS BUFFER 4 TO BE READ BACK IN THE LEAST SIGNIFICANT FOUR BITS (0 TO 3) OF THE 1 K ADDRESS SPACE.

BIT 1 - BUFFER 1(L)/BUFFER 5(H)
A ZERO SELECTS BUFFER 1 A ONE SELECTS BUFFER 5 TO BE READ BACK IN BITS 4 TO 7 OF THE 1 K ADDRESS SPACE.

BIT 2 - BUFFER 2(L)/BUFFER 6(H)
A ZERO SELECTS BUFFER 2 A ONE SELECTS BUFFER 6 TO BE READ BACK IN BITS 8 TO 11 OF THE 1 K ADDRESS SPACE.

BIT 3 - BUFFER 3(L)/BUFFER 7(H)
A ZERO SELECTS BUFFER 3 A ONE SELECETS BUFFER 7 TO BE READ BACK IN BITS 12 TO 15 OF THE 1K ADDRESS SPACE.

BITS 4 TO 7 - QUADRANT CONTROL
THIS 'NIBBLE' SELECTS THE TIMING INPUT FOR THE QUADRANT DIVISION OF THE SCREEN. IT ALSO PERMITS 'FORCING' THE QUADRANT LINES TO A FIXED LOGIC LEVEL, DETERMINED BY BITS 4 AND 5. WHEN BITS 6 AND 7 ARE BOTH LOW, THEY ENABLE NORMAL QUADRANT MODE, BUT WHEN HIGH THEY ENABLE MANUAL CONTROL OVER QUADRANTS BY BITS 4 AND 5:

BIT 6	BIT 7	
Ø	Ø	NORMAL QUADRANT MODE
Ø	1	NOT USED
1	Ø	NOT USED
1	1	QUADRANTS SELECTED BY BITS 4 AND 5

WHEN BITS 6 AND 7 = 1:

BIT 4	BIT 5	
Ø	Ø	QUADRANT Ø
Ø	1	QUADRANT 1
1	Ø	QUADRANT 2
1	1	QUADRANT 3

WHEN BITS 4 AND 5 ARE ENABLED, QUADRANT INFORMATION (B-BUS REQUEST OUTPUT DISPLAY) ARE TIED TO THE CORRESPONDING REGISTERS
EXAMPLE: BIT 6=1, BIT 7=1, BIT 4=Ø, BIT 5=Ø
B-REQUEST QUADRANT Ø (REGISTER 164050) NOW CONTAINS B-BUS REQUEST, OUTPUT DISPLAY QUADRANT Ø (REGISTER 164000) NOW SELECTS OUTPUT FOR THE ENTIRE SCREEN

BITS 8 TO 15 - UNUSED

DISCNAME: 0
FILENAME: PRISRE
UPDATED: 24-NOV-80

THIS PART OF REGISTER IS ACTIVE ONLY WHEN BIT 15 IS SET

PRIORITY/SOFT REQUEST REGISTER

REGISTERS 164060-164076
UPPER BYTE:

15	14	13	12	11	10	9	8
SOFT REQUEST	FORCED WRITE	CONTROL SELECT		DATA SELECT		ADDRESS SELECT	

BIT 15 - SOFT REQUEST
WHEN SET, THIS BIT CAUSES ALL BUFFER MULTIPLEXERS TO BE SELECTED BY THE CONTENTS OF THIS REGISTER. THE PRIORITY LOGIC IS IGNORED DURING A SOFT REQUEST AND THE BUS GRANT SIGNALS ARE DETERMINED BY THE CONTROL SELECT BITS 12 AND 13. WHEN THIS BIT IS ZERO, BUS SELECTION IS DETERMINED BY THE PRIORITY LOGIC AND THE BUS PRIORITY REGISTER (THE LOWER BYTE OF THIS REGISTER).

BIT 14 - FORCED WRITE
THIS IS A SPECIAL BIT ONLY TAKES EFFECT WHEN CONTROL BIT 12 AND 13 ARE SET TO ZERO (CPU). WHEN SET, CONTINUOUS WRITE CYCLES ARE GENERATED, FOR ACQUIRING A REAL TIME IMAGE. THIS WOULD BE A SOFT REQUEST WITH A FORCED WRITE, CONTROL SET TO CPU (00), ADDRESS SET TO X-Y (01) AND DATA SET TO EXTERNAL (01). THIS BIT SHOULD BE LEFT AT ZERO FOR NORMAL CPU READ/WRITE OPERATIONS.

BITS 12 AND 13 - CONTROL SELECT
THESE BITS SELECT THE CONTROL BUS CONNECTED TO THE BUFFER CONTROL INPUTS. BUSES ARE ASSIGNED BY PLACING THE BIT PATTERNS INDICATED IN TABLE ONE INTO THESE BIT POSITIONS. PLACING THESE TWO BITS AT ZERO INVOKES A SPECIAL CPU MODE. THE BUFFER IS PLACED IN A CONTINUOUSLY ENABLED STATE, WITH BIT 14 DETERMINING THE TYPE OF BUFFER CYCLE. WHEN BIT 14 IS ZERO, CONTINUOUS READ CYCLES ARE GENERATED BUT SET TO ONE, A CONTINUOUS WRITE CYCLES ARE INITIATED. THIS PERMITS INTERCONNECTION TO DEVICES THAT DO NOT HAVE THE READ/WRITE AND ENABLE CONTROL LINES, AS IN A 'BARE BONES' X-Y ADDRESSING SCHEME.

BITS 10 AND 11 - DATA SELECT
THESE BITS DETERMINE THE BUS USED FOR BUFFER DATA INPUT. BUSES ARE ASSIGNED TO THIS SELECTOR BY PLACING THE CODE INDICATED IN TABLE ONE INTO THESE BIT POSITIONS.

BITS 8 AND 9 - ADDRESS SELECT
DURING A SOFT REQUEST, ADDRESS SELECTION IS DETERMINED BY PLACING THE CODES INDICATED IN TABLE ONE INTO THESE BIT POSITIONS.

BIT ASSIGNMENT FOR CONTROL, DATA AND ADDRESS SELECT GROUPS:

TABLE ONE:
---

00 - A-BUS (CPU)
01 - B-BUS (XY/EXTERNAL)
10 - C-BUS (PIXEL PROCESSOR)
11 - D-BUS (PIXEL PROCESSOR)

REGISTERS 164060-164076
LOWER BYTE:

7	6	5	4	3	2	1	0
PRIORITY LEVEL #3 (HIGHEST)		PRIORITY LEVEL #2		PRIORITY LEVEL #1		PRIORITY LEVEL #0 (LOWEST)	

REGISTER DESCRIPTION:

THIS REGISTER IS ACTIVE WHEN THE DEVICE ENTERS INTO ITS AUTONOMOUS STATE AND IS USED TO ALLOCATE USAGE OF A BUFFER BY PRIORITIZING OF THE REQUEST/GRANT SEQUENCE. WHEN TWO OR MORE DEVICES REQUEST USE OF A BUFFER (ON DIFFERENT BUSES) SIMULTANEOUSLY, THE CONFLICT IS RESOLVED BY ISSUING A GRANT TO THE DEVICE ASSIGNED THE HIGHEST PRIORITY. IF THE SAME BUS IS SET TO TWO PRIORITY POSITIONS, THE HIGHEST PRIORITY ASSIGNED TO THAT BUS IS IN EFFECT.

EXAMPLE: BUS A (00) IS PLACED AT PRIORITY LEVEL ZERO AND PRIORITY LEVEL TWO. THE HIGHEST PRIORITY IS IN EFFECT (PRIORITY LEVEL TWO).

IF A BUS IS NOT ASSIGNED TO A PRIORITY LEVEL, IT IS EFFECTIVELY LOCKED OUT OF ACCESS TO THAT BUFFER. REQUESTS ON THAT BUS ARE IGNORED, UNTIL ITS PRIORITY IS RE-ESTABLISHED OR A SOFT REQUEST FOR THAT BUS IS ACTIVATED.

BITS 6 AND 7 - PRIORITY LEVEL THREE (THE HIGHEST)
BITS 4 AND 5 - PRIORITY LEVEL TWO (THE SECOND HIGHEST)
BITS 2 AND 3 - PRIORITY LEVEL ONE - THE THIRD HIGHEST PRIORITY
BITS 0 AND 1 - PRIORITY LEVEL ZERO - THE LOWEST PRIORITY LEVEL.

BUSES ARE PLACED AT ANY OF THESE PRIORITY LEVEL BY PLACING THE NUMBERS IN TABLE TWO INTO THESE BIT POSITIONS:

TABLE TWO:
---

00 - A-BUS (CPU)
01 - B-BUS (XY/EXTERNAL)
10 - C-BUS (VIDEO PROCESSOR PORT A)
11 - D-BUS (VIDEO PROCESSOR PORT B)

TITLER

DISCNAME: X
FILENAME: TITLER.DOC
UPDATED: 21-NOV-80

TITLER - OUTPUT KEYER

THE BIT PATTERN CHARACTER ACTS AS A KEY SOURCE TO A TWO INPUT SWITCH. THE TWO INPUTS ARE IDENTIFIED AS THE A- AND B-INPUT. THE A-INPUT CAN BE FURTHER SELECTED FROM TWO INPUTS:

1) THE A-MATTE REGISTER
2) THE EXTERNAL A-INPUT

EACH OF THESE INPUTS ARE 12 BITS WIDE, CORRESPONDING TO FOUR BITS ON RED, GREEN AND BLUE.

THE A-MATTE REGISTER IS USED TO HOLD THE 'BACKGROUND' COLOR INTO WHICH THE CHARACTER IS KEYED. THE EXTERNAL A-INPUT ALLOWS THE BACKGROUND TO BE ORIGINATED FROM ANOTHER 12 BIT SOURCE.

THE B-INPUT SIDE OF THE OUTPUT KEYER SELECTS BETWEEN ONE OF FOUR SOURCES. THESE SOURCES ARE 'INSERTED' INTO THE 'KEY' GENERATED BY THE CHARACTER.

THE FOUR SOURCES ARE:

1) THE B- MATTE REGISTER
2) THE COLOR MAP
3) THE EXTERNAL B-INPUT
4) ~~UNUSED~~ USED AS (PYCIRTHUR) DIRECT TEST INPUT PORT (SEE BACKPLANE FOR PIN ASSIGNMENTS)

THE B-MATTE REGISTER DEFINES A 12 BIT NUMBER THAT IS OUTPUT DURING THE CHARACTER KEY. THIS VALUE IS KEYED INTO THE BACKGROUND, SELECTED BY THE A-INPUT.

THE COLOR MAP IS A 256 WORD BY 12 BIT COLOR MAP. IT MAPS 8 BITS OF THE CHARACTER CODE INTO 256 TWELVE BIT COLORS. IF SELECTED, THIS COLOR IS KEYED INTO THE BACKGROUND (SEE FURTHER EXPLANATION UNDER 'COLOR MAP').

THE EXTERNAL B-INPUT MAY BE SELECTED TO KEY IN AN EXTERNAL IMAGE, SUPPLIED BY THE 'EXTERNAL B-INPUT' PINS. THIS INPUT IS USEFUL IF THE CHARACTER IS TO CONTAIN A 'TEXTURE', WHICH THEN IS SUPPLIED BY THIS 'EXTERNAL (B-INPUT) SOURCE'.

ALPHANUMERIC CHARACTERS ARE DISPLAYED IN AN 8 BY 12 GRID, OF WHICH 7X9 OF THESE ARE OCCUPIED BY THE CHARACTER DOT PATTERN. THE TOP ROW IS ALWAYS BLANK, THE NEXT 9 ROWS (1-9), ARE OCCUPIED BY UPPER CASE CHARACTERS. A SPECIAL FORMAT IS USED FOR THE 5 DESCENDER CHARACTERS (G, J, P, G, Y). THESE FIVE ARE DESCENDED 2 LINES TO OCCUPY ROWS 3-11, WITH ROWS 1 AND 2 BLANK.

THE ALPHANUMERIC FONT DISPLAY MAY BE EXCHANGED FOR FOUR SETS OF PROGRAMMABLE FONTS, STORED IN THE SCRATCHPAD MEMORY. THE STORED FONT REPRESENTS AN 8H X 16V ARRAY OF DOTS. EACH FONT SET OCCUPIES 2K (2048) BYTES OF SCRATCHPAD MEMORY WITH THE 2K EQUALS 16 ROWS PER FONT BY 128 FONTS. THESE 128 FONTS CONSTITUT ONE 'FONT SET'.

THE 8 BITS PER ROW ARE DISPLAYED ON THE SCREEN; LSB TO THE LEFT SIDE MSB TO THE RIGHT OF FONT. THE FONT SETS ARE STORED IN SCRATCHPAD PAGES (EXTENDED ADDRESS REGISTER 164114), 8 TO 11, AND WRITTEN TO THROUGH ADDRESSES 160000-163776.

FOR EACH FONT, THE SIXTEEN ROWS ARE STORED IN SIXTEEN SEQUENTIAL BYTES OF THE SCRATCHPAD MEMORY, TOP ROW (ROW 0) IS AT THE LOWEST ADDRESS OF THE 16 BYTES.

PAGE 8

FONT 0	BITS 0-7	ASCII CODES 0-63
FONT 1	BITS 8-15	ASCII CODES 0-63

PAGE 9

FONT 0	BITS 0-7	ASCII CODES 64-127
FONT 1	BITS 8-15	ASCII CODES 64-127

PAGE 10

FONT 2	BITS 0-7	ASCII CODES 0-63
FONT 3	BITS 8-15	ASCII CODES 0-63

PAGE 11

FONT 2	BITS 0-7	ASCII CODES 64-127
FONT 3	BITS 8-15	ASCII CODES 64-127

CHARACTER MEMORY

THE 256 CHARACTERS ARE STORED IN A 256 WORD BY 28 BIT DEEP CHARACTER MEMORY. THESE MEMORY BITS ARE ASSIGNED AS FOLLOWS:

CHARACTER MEMORY BITS 0-15

THESE BITS ARE ACCESSED THROUGH MEMORY LOCATIONS 160000-160776, AND PAGE REGISTER SET TO 15. (CLEAR BIT 3 IN REGISTER 164120)

PAGE REGISTER 164114 = 15. (BITS 0-15)
LOWER WORD:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR							FONT	ASCII FONT BITS							

BITS 0-7

1) ASCII CODE WHEN IN 'CHARACTER MODE'
   BITS 0-6 STORE THE ASCII CODE
   IN ALPHANUMERIC MODE, BIT 7 IS UNUSED
2) BIT PATTERN FOR 'THIN GRAPHICS' LINE MODE
3) BIT PATTERN WHEN IN 'WIDE GRAPHICS' MODE
4) PROGRAMMED FONT
   BITS 0-6 SELECT 1 OF 128 FONTS
   BIT 7 SELECTS FONT #1 OR #2

(SEE MODE BITS FOR FURTHER EXPLANATION OF FONTS)

BITS 8-15

THESE 8 BITS DEFINE THE COLOR ASSIGNED THROUGH THE COLOR MAP

CHARACTER MEMORY BITS 16-27

THESE BITS ARE ACCESSED THROUGH MEMORY LOCATIONS 161000-161776, AND PAGE REGISTER SET TO 15.

PAGE REGISTER 164114 = 15. (BITS 16-27)
UPPER WORD:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		CURSOR	REVERSE VIDEO	UNDERLINE	STRIKE THROUGH	BLINK	FONT	MODE1	MODE0	H SPACE					

BITS 0-3
THESE FOUR BITS DEFINE INTERCHARACTER SPACING ALONG THE HORIZONTAL AXIS. SPACES ARE INSERTED AT THE RIGHT EDGE OF THE CHARACTER.
THE SPACE 'WIDTH' IS DETERMINED BY THE CURRENT HORIZONTAL SIZE.

DISPLAY MODE BITS 4-7

BIT 4 MODE SELECT 0
BIT 5 MODE SELECT 1
BIT 6 FONT SELECT

FONT(H)	MODE1	MODE0 (BITS 6-4)	
0	0	0	WIDE GRAPHIC
0	0	1	ASCII VERTICAL STRIPE GRAPHIC
0	1	0	THIN GRAPHIC
0	1	1	ALPHANUMERIC-INTERNAL CHARACTER
1	0	X	FONT LOW - PROGRAMMED (LOWER 8 BITS)
1	1	X	FONT HIGH - PROGRAMMED (UPPER 8 BITS) (OF SCRATCHPAD)

NOTE: WHEN HIGH, THE SIXTH BIT INTERACTS WITH "FONT" BIT 7

0 = LOW, 1 = HIGH, X = DON'T CARE

BIT 7 BLINK
WHEN THIS BIT IS SET THE CHARACTER WILL BLINK. THE RATE OF THE BLINK IS CONTROLLED BY THE BLINK-RATE REGISTER

BIT 8 - STRIKE THROUGH
WHEN SET THE DISPLAYED CHARACTER WILL HAVE A HORIZONTAL LINE 'STRUCK THROUGH' THE CHARACTER

BIT 9 - UNDERLINE
WHEN SET, THE CHARACTER WILL BE UNDERLINED

BIT 10 - REVERSE VIDEO
WHEN SET, THE 'CHARACTER CELL' WILL CONTAIN A REVERSAL OF FOREGROUND/BACKGROUND

BIT 11 - CURSOR
WHEN SET, A CURSOR WILL APPEAR AT THE CHARACTER. THE CURSOR FORMAT IS AFFECTED BY BITS 7-10

TO OPERATE/ TEST INPUT (B-IN)
SET KEYPOL (BIT 11) TO 1 AND
BIT 1,2 (B-IN) TO HIGH (OCTAL 4006)

FOR OVERLAY
FILL 164120
4511

TITLER REGISTERS

WHILE MOST OPERATIONS ON CHARACTERS ARE DEFINED THROUGH THE CHARACTER RAM, CERTAIN PARAMETERS ARE SET UP BY REGISTERS. THESE REGISTERS ARE:

CONTROL REGISTER 164120

THIS REGISTER IS USED FOR SWITCH-OVER OF SELECTIONS AND CONTROL BITS OF THE TITLER

11	10	9	8	7	6	5	4	3	2	1	0
KEY POL	COLOR MAP SELECT KEY		SCRATCH IN SELECT	COLOR MAP SELECT	CHAR RAM.	B-IN SEL			A-IN SEL		

BIT 0 A-INPUT SELECT (OUTPUT KEYER)

BIT 0	
0	A-MATTE INPUT
1	A-EXTERNAL INPUT

BITS 1-2 B-INPUT SELECT (OUTPUT KEYER)

BIT 2	BIT1	
0	0	B-MATTE REGISTER
0	1	COLOR MAP
1	0	EXTERNAL B-INPUT
1	1	UNUSED

BIT 3 CHARACTER RAM ADDRESS SELECT

BIT 3	
0	LSI-11 (ALLOWS WRITING OF CHARACTER RAM BY LSI=11
1	TITLER TIMING

BITS 4-5 COLOR MAP ADDRESS SELECT

BIT 5	BIT 4	
0	0	LSI-11
0	1	CHARACTER RAM
1	0	EXTERNAL B-INPUT
1	1	UNUSED

BITS 6-7 SCRATCH-PAD INPUTS SELECT:

BIT 7	BIT 6	
0	0	LSI-11
0	1	CHARACTER RAM
1	0	C-BUS
1	1	C-BUS

BITS 8-10 KEY SELECT

THIS REGISTER CHOOSES ONE OF EIGHT BITS TO ACT AS THE OUTPUT KEY. THE MSB SELECTS AN INVERTED/NONINVERTED KEY. THESE BITS ARE:

BIT 10	BIT 9	BIT 8	
0	0	0	CHARACTER KEY (BORDERS BLANK)
0	0	1	CHARACTER KEY (SPILL OVER BORDERS)
0	1	0	CHARACTER KEY UNBLANKED
0	1	1	KEY INVERT(L) (0=INVERT, 1=NON-INVERT)
1	0	0	UNUSED
1	0	1	CHARACTER TITLING BORDER
1	1	0	BUFFER OUTPUT 0 MSB
1	1	1	'TRUE'

BIT 11 KEY INVERT BIT

BIT 11	
0	INVERT
1	NON-INVERT

HORIZONTAL/VERTICAL SIZE REGISTER 164122

7	6	5	4	3	2	1	0
HORIZONTAL SIZE				VERTICAL SIZE			

THIS REGISTER DETERMINES THE NUMBER OF PIXELS OCCUPIED BY EACH CHARACTER DOT:

BITS 0-3 VERTICAL SIZE ;0 LARGEST, 15 SMALLEST
BITS 4-7 HORIZONTAL SIZE ;0 LARGEST, 15 SMALLEST
BITS 8-11 VERTICAL SPACING ;0 LARGEST, 15 CLOSEST

SETS UP THE VERTICAL SPACING BETWEEN CHARACTER ROWS, VARYING ON A SCALE FROM 0 TO 15, WHERE 0 = NO SPACE. THE SPACING IS AFFECTED BY THE VERTICAL SIZE REGISTER, AND IS PROPORTIONAL TO THE SIZE

BITS 12-15 BLINK RATE REGISTER

DETERMINES THE RATE OF BLINKING AND BLINKING CURSOR CHARACTERS. THE BLINK RATE VARIES FROM 1/15TH TO 1 SECOND

TITLING WINDOW

REGISTER 164124 (TOP LEFT)

```
+-------------------------------+-------------------------------+
!15 !14 !13 !12 !11 !10 ! 9 ! 8 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0!
+-------------------------------+-------------------------------+
!               X1              !               Y1              !
```

REGISTER 164126 (BOTTOM RIGHT)

```
+-------------------------------+-------------------------------+
!15 !14 !13 !12 !11 !10 ! 9 ! 8 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0!
+-------------------------------+-------------------------------+
!               X2              !               Y2              !
```

X1 LEFT EDGE: 0 — Y1 TOP EDGE: ?
X2 RIGHT EDGE: 177 — Y2 BOTTOM EDGE: ?

A - MATTE, REGISTER 164130

BITS 0-3	RED
BITS 4-7	GREEN
BITS 8-11	BLUE
BITS 12-15	UNUSED

B - MATTE, REGISTER 164132

BITS 0-3	RED
BITS 4-7	GREEN
BITS 8-11	BLUE
BITS 12-15	UNUSED

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

D76A

DISCNAME: X
FILENAME: DTOA.DOC
UPDATED: 24-NOV-80

DIGITAL TO ANALOG CONTROL REGISTERS

D TO A MAP INPUT/OUTPUT FORMAT:

REGISTER 164134

EXTRA		BLU		GREEN		RED	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS1	OS0	MS1	MS0	OS1	OS0	MS1	MS0	OS1	OS0	MS1	MS0	OS1	OS0	MS1	MS0

MAP ADDRESS TABLE:

MSEL 1	MSEL 0	
0	0	LSI-11
0	1	8 BIT MAP
1	0	6 BIT MAPS (1 OF 4) [FURTHER SELECTED BY
1	1	4 BIT MAPS (1 OF 16) REGISTER 164136]

NOTE: TO ACTIVATE THESE BITS, THE "MAPPED OUTPUT" BITS (SEE TABLE BELOW) MUST BE SET.

OUTPUT FORMAT TABLE:

OSEL 1	OSEL 0	
0	0	8 BIT DIRECT
0	1	6 BIT DIRECT
1	0	4 BIT DIRECT
1	1	MAPPED OUTPUT (SEE MAP SELECT TABLE ABOVE)

THE 4- AND 6- BIT COLOR MAPS ARE FURTHER SELECTED THROUGH THE 'COLOR MAP SELECTION REGISTER'

COLOR MAP SELECTION REGISTER

REGISTER 164136

EXTRA				BLU				GREEN				RED			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S3	S2	S1	S0	S3	S2	S1	S0	S3	S2	S1	S0	S3	S2	S1	S0

IN 4 BIT MAP MODE S0-S3 REPRESENTS 0-15 (COLOR MAPS 0-15)
IN 6 BIT THIS TABLE APPLIES:

S3	S2	S1	S0	
0	0	X	X	MAP 0
0	1	X	X	MAP 1
1	0	X	X	MAP 2
1	1	X	X	MAP 3
etc				etc

WHERE: 0 = LOW 1 = HIGH AND X = DON'T CARE
WHEN # 14. IS PLACED IN THE PAGE REGISTER(164114 = 14.)
THIS MEMORY ASSIGNMENT BECOMES ACTIVE:

COLOR MAP: 160000-160776
LOW BYTE - RED 8 BIT MAP LSB = 0
HIGH BYTE - GREEN 8 BIT MAP LSB = 8
COLOR MAP: 161000-161776
LOW BYTE - BLUE 8 BIT MAP LSB = 0
HIGH BYTE - EXTRA 8 BIT MAP LSB = 8

SUMMARY:

DISCNAME: X
FILENAME: SEQREG.DOC
UPDATED: 26-NOV-80

MICSTA CONTROL STORE

ALU/SEQUENCER MICRO-DEVICE REGISTERS

ADDRESS = 164140 MICRO CONTROL STATUS REGISTER
- BIT 0 - RUN(L)/HALT READ/WRITE
- BIT 1 - CLOCK STOPPED(L), SINGLE STEP<WRITE ONLY>
- BIT 2 - PIPELINE SINGLE STEP ENABLE
- BIT 3 - ALU/SEQ/REGISTER SINGLE STEP ENABLE
- BIT 4 - ADDRESS FORCE
- BIT 5 - LSI-11 TEST CONDITION BIT TST1
- BIT 6 - LSI-11 TEST CONDITION BIT TST2
- BITS 7-13 ~~- UNUSED~~ 7 TO 9 SUBROUTINE TST CONDITIONES 10 TO 13 UNUSED
- BIT 14 - MEMORY TRAP 'BLOCK'
- BIT 15 - MEMORY TRAP

ADDRESS =164142 MICRO ADDRESS
- BIT 0 TO 11 - MICROADDRESS BITS
- BIT 12 TO 15 - UNUSED

CONTROL STORE WRITE / PIPELINE READ GROUPS 0-5

NOTE: THE LOWEST NUMBER OF EACH REGISTER IS THE LEAST SIGNIFICANT BIT.

ADDRESS = 164144 GROUP 0 DATA REGISTER BITS 0 TO 15
ADDRESS = 164146 GROUP 1 DATA REGISTER BITS 16 TO 31
ADDRESS = 164150 GROUP 2 DATA REGISTER BITS 32 TO 47
ADDRESS = 164152 GROUP 3 DATA REGISTER BITS 48 TO 63
ADDRESS = 164154 GROUP 4 DATA REGISTER BITS 64 TO 79
ADDRESS = 164156 GROUP 5 DATA REGISTER BITS 80 TO 95

THE GROUP 5 DATA REGISTER (164156) IS NOT ACTIVE IN THE PRESENT SYSTEM.

ADDRESS = 164160 SEQUENCER STATUS
- BIT 0 - SEQUENCER CONDITION CODE TEST BIT
- BIT 1 - SEQUENCER STACK FULL
- BITS 2-15 - UNUSED

ADDRESS = 164162 SEQUENCER 'DIRECT' INPUT REGISTER
- BITS 0-11 - SEQUENCER DIRECT INPUT
- BITS 12-15 - UNUSED

ADDRESS = 164164 UNUSED

ADDRESS = 164166 ALU READBACK REGISTER BITS 0-15

DISCNAME: X
FILENAME: SEQCON.DOC
UPDATED: 18-NOV-80

MICRO CONTROL/STATUS REGISTER:

ADDRESS=164140

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
MT	MTB	NU	NU	NU	NU	NU	NU	NU	TST	TST	AF	ASR	SSE	R/S	H/R

BIT DESCRIPTION:

BIT 0 - HALT/RUN(L)
WHEN 'LOW' THE VIDEO PROCESSOR RUNS THE CONTROL STORE PROGRAM, FROM THE CURRENT MICRO-ADDRESS. WHEN ASSERTED, IT STOPS THE VIDEO PROCESSOR CLOCK AND ENABLES BIT 1, 2 AND 3.

BIT 1 - SINGLE STEP CONTROL - RUN/STOP STATUS
THIS BIT FUNCTIONS IN CONJUNCTION WITH BITS 0, 2 AND 3, AND HAS TWO FUNCTIONS; WHEN READ, IT INDICATES IF THE CLOCK HAS 'GROUND TO A HALT'(RUN=1, HALTED=0). WITH THE HALT BIT ASSERTED, EACH 'HIGH' SETTING OF THIS BIT GENERATES A SINGLE STEP OF THE SEQUENCER/ALU CLOCK.

BIT 2 - PIPELINE SINGLE STEP ENABLE
ACTS ALONG WITH BIT 1 TO PASS SINGLE STEPS TO THE PIPELINE REGISTER. WHEN BOTH BITS (1 AND 2) ARE HIGH, THEY CAUSE A STROBING OF THE PIPELINE REGISTER.

BIT 3 - ALU/SEQUENCER REGISTER SINGLE STEP ENABLE
THIS BIT OPERATES ALONG WITH BIT 1 TO PASS SINGLE STEP CLOCKS TO THE ACTIVE UNITS OF THE PROCESSOR: THE INTERNAL REGISTER FILE, Q REGISTER, STATUS LATCH, THE SEQUENCER, AND THE EXTERNAL REGISTERS.

BIT 4 - ADDRESS FORCE;
BIT 4 CAUSES THE CONTROL STORE'S ADDRESS TO COME FROM THE LSI-11 MICRO-ADDRESS REGISTER (BITS 0 TO 11 OF ADDRESS=164142).

BIT 5 - LSI-11 TEST CONDITION BIT TST1

BIT 6 - LSI-11 TEST CONDITION BIT TST2

BITS 7-13 - ~~NOT USED~~

BIT 14 - MEMORY TRAP 'BLOCK'

BIT 15 - MEMORY TRAP

FILENAME: PIPREG.DOC
LISKNAME: L (BACKPLANE)
UPDATED: 1-DEC-79

PIPE

Ø TO MAX

DEC

PIPELINE REGISTER ASSIGNMENT

OCT	REGISTER	HEX		CONTROL/FUNCTION
Ø	REG #164144	Ø	SEQ=	INSTRUCTION BIT Ø
1	(GROUP)	1		INSTRUCTION BIT 1
2		2		INSTRUCTION BIT 2
3		3		INSTRUCTION BIT 3
4		4	POL=	TEST POLARITY
5		5	TST=	TEST SELECT BIT Ø
6		6		TEST SELECT BIT 1
7		7		TEST SELECT BIT 2
8		8		TEST SELECT BIT 3
9		9		TEST SELECT BIT 4
10		A	MTRAP=	MEMORY TRAP(H)
11		B	EMIT=	EMIT BIT Ø
12		C		EMIT BIT 1
13		D		EMIT BIT 2
14		E		EMIT BIT 3
15		F		EMIT BIT 4

WRITING THE CONTROL STORE

THESE ARE STEPS ALONG WITH A SAMPLE PROGRAM IN MACRO ASSEMBLER FOR WRITING THE CONTROL STORE OF THE VIDEO PROCESSOR.

1) IN THE MICRO-CONTROL REGISTER (164140), HALT THE VIDEO PROCESSOR BY SETTING BIT 0 TO A 'HIGH' AND THE SINGLE STEP (BIT 1) TO A 'LOW'. THIS STOPS THE CLOCK AND HOLDS THE CURRENT PIPELINE INSTRUCTION. TEST FOR BIT 1 = LOW BY READING THE MICRO/STATUS REGISTER. WHEN BIT 1 READS BACK AS A 'ZERO', THE CLOCK HAS FULLY STOPPED.

2) ASSERT THE ADDRESS FORCE BIT (BIT 4 OF ADDRESS 164140). NOW THE ADDRESS FOR THE CONTROL STORE COMES FROM THE MICRO-ADDRESS REGISTER (ADDRESS 164142) INSTEAD OF THE SEQUENCER.

3) PLACE THE ADDRESS OF THE CONTROL STORE WORD INTO THE MICRO-ADDRESS REGISTER (ADDRESS 164142, BITS 0 TO 11). THIS ADDRESS POINTS TO AN 80 BIT CONTROL STORE WORD.

4) MOVE OPERATION - DATA WILL NOW BE WRITTEN TO THE CONTROL STORE BY SENDING DATA TO THE APPROPRIATE DATA GROUP REGISTER AS SHOWN BELOW:

DATA GROUP 0	- BITS 0 TO 15 OF CONTROL STORE	ADDRESS 164144
DATA GROUP 1	- BITS 16 TO 31 OF CONTROL STORE	ADDRESS 164146
DATA GROUP 2	- BITS 32 TO 47 OF CONTROL STORE	ADDRESS 164150
DATA GROUP 3	- BITS 48 TO 63 OF CONTROL STORE	ADDRESS 164152
DATA GROUP 4	- BITS 64 TO 79 OF CONTROL STORE	ADDRESS 164154
DATA GROUP 5	- BITS 80 TO 95 OF CONTROL STORE	ADDRESS 164156

5) TO VERIFY THE WRITTEN LOCATION IT IS NECESSARY TO READ THE CONTROL STORE WORD THROUGH THE PIPELINE REGISTER. THE PIPELINE REGISTER IS READ IN FIVE GROUPS OF 16 (SIXTEEN) BITS, FROM THE DATA GROUP REGISTERS 0 TO 4 (THE SIXTH GROUP IS NOT ACTIVE NOW). HOWEVER, BEFORE READING THE DATA GROUP REGISTERS, THE PIPELINE MUST BE STROBED TO PUSH THROUGH THE CURRENTLY ADDRESSED CONTROL STORE WORD. THIS IS DONE BY ENABLING BIT 2 OF THE MICRO-CONTROL REGISTER AND SETTING THE SINGLE STEP BIT 1 TO A 'HIGH', TO INITIATE A SINGLE CLOCK STROBE. TESTING BIT 1 INDICATES WHEN THIS 'STEPPING' IS COMPLETE (BIT 1 = ZERO WHEN THE CLOCK IS STOPPED).

```
**************************************************************
0  REG #164152 0                    B INPUT SELECT 4 INT/EXT
1    (GROUP+6)  1 PFORMAT=          POST-FORMAT ENABLE
2               2 OUT=              ALU OUTPUT SELECT 0
3               3                   ALU OUTPUT SELECT 1
--------------------------------------------------------------
4               4                   ALU OUTPUT SELECT 2
5               5                   ALU OUTPUT SELECT 3
6               6                   ALU OUTPUT SELECT 4
7               7 STATUS=           STATUS HOLD
--------------------------------------------------------------
8               8 ROTATE=           ALU ROTATE 0
9               9                   ALU ROTATE 1
10              A                   ALU ROTATE 2
11              B                   ALU ROTATE 3
--------------------------------------------------------------
12              C SPECIAL=          ALU SPECIAL INSTRUCTION
13              D CADRES=           CLEAR
14              E                   UP/DOWN(L)
15              F                   LOAD/COUNT (L)
**************************************************************
0  REG #164154 0                    ENABLE/HOLD (L)
1  (GROUP+10 ) 1 DADRES=           CLEAR
2              2                   UP/DOWN (L)
3              3                   LOAD/COUNT (L)
--------------------------------------------------------------
4              4                   ENABLE/HOLD (L)
5              5 CCON=             C-BUS ENABLE(L)
6              6                   BUFFER ENABLE (L)          WRITE(L)
7              7                   BUFFER READ/WRITE(L),C-BUS WRITE(L
--------------------------------------------------------------
8              8                   C-BUS READ (L)
9              9 DCON=             BUFFER ENABLE(L)
10             A                   BUFFER READ(H)/WRITE(L)
11             B RANDOM=           RANDOM CONTROL 0
--------------------------------------------------------------
12             C                   RANDOM CONTROL 1
13             D EXTRA=            EXTRA
14             E                   EXTRA
15             F                   EXTRA
**************************************************************
```

```
**************************************************************
**************************************************************
 0  REG #164146 0                  EMIT BIT 5
 1    (GROUP+2)  1                  EMIT BIT 6
 2               2                  EMIT BIT 7
 3               3                  EMIT BIT 8
--------------------------------------------------------------
 4               4                  EMIT BIT 9
 5               5                  EMIT BIT 10
 6               6                  EMIT BIT 11
 7               7                  EMIT BIT 12
--------------------------------------------------------------
 8               8                  EMIT BIT 13
 9               9                  EMIT BIT 14
 10              A                  EMIT BIT 15
 11              B IDLE=            ALU IDLE
--------------------------------------------------------------
 12              C IZERO=           ALU INSTRUCTION BIT 0
 13              D ALU=             ALU INSTRUCTION BIT 1
 14              E                  ALU INSTRUCTION BIT 2
 15              F                  ALU INSTRUCTION BIT 3
**************************************************************
 0  REG #164150 0                  ALU INSTRUCTION BIT 4
 1    (GROUP+4)  1 SHIFTER=        ALU INSTRUCTION BIT 5
 2               2                  ALU INSTRUCTION BIT 6
 3               3                  ALU INSTRUCTION BIT 7
--------------------------------------------------------------
 4               4                  ALU INSTRUCTION BIT 8
 5               5 CARRYIN=         ALU CARRY IN
 6               6 AIN=             A INPUT SELECT 0
 7               7                  A INPUT SELECT 1
--------------------------------------------------------------
 8               8                  A INPUT SELECT 2
 9               9                  A INPUT SELECT 3
 10              A                  A INPUT SELECT 4
 11              B                  A INPUT SELECT 5 INT/EXT
--------------------------------------------------------------
 12              C BIN=             B INPUT SELECT 0
 13              D                  B INPUT SELECT 1
 14              E                  B INPUT SELECT 2
 15              F                  B INPUT SELECT 3
**************************************************************
```

INT REG

DISCNAME: 0
FILENAME: SEQUEN
UPDATED: 24-NOV-79

SEQ TST'S

T H E S E Q U E N C E R C O N T R O L G R O U P

DESCRIPTION AND OPERATION:

THE SEQUENCER IS RESPONSIBLE FOR CO-ORDINATING THE OUTPUTS OF THE OTHER CONTOL STORE GROUPS, BY CHOOSING WHICH CONTROL STORE WORD SHOULD BE READ OUT TO THE PIPELINE REGISTER, AND THEN EXECUTED. THIS CHOICE IS MADE BY OUTPUTTING AN ADDRESS TO THE WRITEABLE CONTROL STORE, ACCESSING THE ADDRESSED CONTROL WORD.

THE MICROPROGRAM SEQUENCER SETS THE SPEED OF INSTRUCTION EXECUTION BY READING OUT CONTROL STORE LOCATIONS AND SENDING THEM TO THE PIPELINE REGISTER. THE PIPELINE REGISTER IS USED TO HOLD THE CONTROL STORE OUTPUT UNTIL ANOTHER CONTROL STORE WORD IS AVAILABLE. THE SPEED OF ACCESSING THE CONTROL STORE HAS BEEN SET TO 200 NANOSECONDS WHICH IS ALSO THE OPERATING SPEED OF THE IMAGE BUFFERS AND THE ARITHMETIC UNIT. ALL CHANGES OR OPERATIONS MUST CONFROM TO THIS SPEED OR CYCLE TIME, IF THEY ARE TO BE CONTROLLED BY THE VIDEO PIXEL PROCESSOR.

THE MICROPROGRAM SEQUENCER USED IS AN AMD (ADVANCED MICRO DEVICES) 2910. IT ALLOWS ADDRESSING OF UP TO 4096 CONTROL STORE LOCATIONS, OF WHICH ONLY 256 ARE CURRENTLY UTILIZED (THERE ARE TWO PAGES OF 256 WORDS). THE 2910 DETERMINES THE CONTROL STORE ADDRESS OR LOCATION, BY ITS CURRENT INSTRUCTION. THERE ARE SIXTEEN POSSIBLE INSTRUCTIONS, SOME OF WHICH ARE CONDITIONALLY EXECUTED. THE FOUR BIT 'SEQUENCER INSTRUCTION' GROUP IS USED TO DECIDE WHICH INSTRUCTION TO EXECUTE. THE CURRENT PIPELINE WORD DECIDES THE NEXT CONTROL LOCATION BY THE INSTRUCTION GROUP, TEST CONDITION GROUP, AND FOR CERTAIN INSTRUCTIONS THE 'EMIT' GROUP. WE WILL NOW PURSUE THE SEQUENCER INSTRUCTION SET AND ITS USAGE IN A MICROPROGRAM:

0000--INSTRUCTION ZERO IS JUMP TO ZERO OR RESET INSTRUCTION. IT IS USED TO FORCE MICROPROGRAM EXECUTION AT LOCATION ZERO OF THE CONTROL STORE. IT IS ALSO FORCED BY THE LSI-11 TO BEGIN EXECUTING A MICROPROGRAM, AFTER IT HAS BEEN LOADED INTO THE CONTROL STORE. THIS INSTRUCTION ALSO RESETS THE STACK POINTER.

FOR A TABLE OF INSTRUCTIONS, SEE THE DESCRIPTION OF THE AMD 2910 CHIP.

DISCNAME: X
FILENAME: TESSEL.DOC
UPDATED: 24-NOV-80

SEQUENCER TEST SELECT/POLARITY CONTROL STORE GROUP

POLARITY

THIS BIT CONTROLS THE POLARITY OF A TEST CONDITION. WHEN ZERO, THE CONDITION IS PASSED ON TO THE SEQUENCER IN ITS NON-INVERTED FORM. WHEN SET, THE SELECTED TEST CONDITION IS INVERTED BEFORE BEING SENT ALONG TO THE SEQUENCER TEST INPUT. THIS BIT IS USEFUL FOR TESTING 'REVERSE' TEST CONDITIONS. FOR EXAMPLE, WHEN TESTING FOR A 'NOT ZERO' RESULT OF A PREVIOUS ALU OPERATION, THE POLARITY BIT IS USED AS FOLLOWS: THE TEST CONDITION BIT IS ENABLED, THE TEST CONDITION SELECT IS SWITCHED TO THE 'ZERO' TEST CONDITION, AND THE POLARITY OF THE TEST IS SET (INVERTED). IF THE PREVIOUS TEST CONDITION WAS NOT ZERO, THE RESULT OF THIS TEST WOULD BE TRUE (ZERO INVERTED EQUALS NOT ZERO). THIS BIT ALSO CONSIDERS THE POLARITY OF EXTERNAL TEST SIGNALS. WHEN SET, THE NEGATIVE LEVEL OF THE TESTED SIGNAL IS CONSIDERED A TRUE TEST CONDITION, AND WHEN RESET, THE POSITIIVE LEVEL OF THE TESTED CONDITION IS CONSIDERED A TRUE TEST INPUT.

TEST CONDITION SELECT BITS

THIS CONTROL STORE GROUP DETERMINES WHICH TEST INPUT IS PASSED ALONG TO THE SEQUENCER TEST INPUT.

TEST CONDITIONS

POL
98765 = (P9-P8-P7-P6-P5)

00000	0H	TRUE	TRUE
00001	1H	LSI-11- TST I	LSI-11 TST1
00010	2H	LSI-11- TST II	LSI-11 TST2
00010	3H	HD	UNASSIGNED
00011	4H	VD	H DRIVE
00100	5H	C-MATCH	V DRIVE
00101	6H	D-MATCH	C-MATCH(L)
00110	7H	BLANKING	D-MATCH(L)
00111	8H	EXTRA	BLANKING
8-17	8-18H		UNUSED

BINARY HEX DEC POL=PIPELINE BIT #4

11000	18H	24	INV	(NEGATIVE (EX/OR) OVERFLOW) + ZERO
11001	19H	25	INV	(NEGATIVE (EX/OR) OVERFLOW)
11010	1AH	26	INV	ZERO
11011	1BH	27	INV	OVERFLOW
11100	1CH	28	INV	CARRY + ZERO
11101	1DH	29	INV	CARRY
11110	1EH	30	INV	CARRY(L) + ZERO
11111	1FH	31	INV	NEGATIVE
11000	18H	24	POS	(NEGATIVE (EX/NOR) OVERFLOW) - ZERO
11001	19H	25	POS	(NEGATIVE (EX/NOR) OVERFLOW)
11010	1AH	26	POS	ZERO(L)
11011	1BH	27	POS	OVERFLOW(L)
11100	1CH	28	POS	CARRY(L) . ZERO(L)
11101	1DH	29	POS	CARRY(L)
11110	1EH	30	POS	CARRY . ZERO(L)
11111	1FH	31	POS	NEGATIVE(L)

TRUE TEST CONDITION

ALU STATUS REGISTER: AMD 2910
POLARITY = NON-INVERTED (0)
TEST SELECT = 0

THIS INPUT SETS THE TEST INPUT TO TRUE, FORCING EXECUTION OF CONDITIONAL SEQUENCER INSTRUCTIONS. THIS IS USEFUL WHEN TEST CONDITIONS ARE TO BE IGNORED, AND WHEN ATTEMPTING TO EXECUTE CONDITIONAL INSTRUCTIONS UNCONDITIONALLY. EXAMPLE: CJS (CONDITIONAL JUMP-TO-SUBROUTINE) WITH CONDITION CODE SET AT 'TRUE' BECOMES A JUMP-TO-SUBROUTINE INSTRUCTION. IF THE POLARITY BIT IS SET TO 'INVERT', THIS INPUT IS A 'FALSE' INPUT, CAUSING ALL CONDITIONAL SEQUENCES TO FAIL.

SEE AMD 2904 DESCRIPTION: STATUS AND SHIFT CONTROL UNIT (PAGE 4, TABLE 4) (PUB077) 1978

TEST CONDITIONS

POL
98765 = (P9-P8-P7-P6-P5)

00000	0H	TRUE
00001	1H	LSI-11 TST1
00010	2H	LSI-11 TST2
00010	2H	UNASSIGNED
00011	3H	H DRIVE
00100	4H	V DRIVE
00101	5H	C-MATCH(L)
00110	6H	D-MATCH(L)
00111	7H	BLANKING
8-17H	UNUSED	
11000	18H	(NEGATIVE (EX/OR) OVERFLOW) + ZERO
11001	19H	(NEGATIVE (EX/OR) OVERFLOW)
11010	1A	ZERO
11011	1B	OVERFLOW
11100	1C	CARRY + ZERO
11101	1D	CARRY
11110	1E	CARRY(L) + ZERO
11111	1F	NEGATIVE
11000	30	(NEGATIVE (EX/NOR) OVERFLOW) - ZERO
11001	31	(NEGATIVE (EX/NOR) OVERFLOW)
11010	32	ZERO(L)
11011	33	OVERFLOW(L)
11100	34	CARRY(L) . ZERO(L)
11101	35	CARRY(L)
11110	36	CARRY . ZERO(L)
11111	37	NEGATIVE(L)

TRUE TEST CONDITION

ALU STATUS REGISTER: AMD 2910
POLARITY = NON-INVERTED (0)
TEST SELECT = 0

THIS INPUT SETS THE TEST INPUT TO TRUE, FORCING EXECUTION OF CONDITIONAL SEQUENCER INSTRUCTIONS. THIS IS USEFUL WHEN TEST CONDITIONS ARE TO BE IGNORED, AND WHEN ATTEMPTING TO EXECUTE CONDITIONAL INSTRUCTIONS UNCONDITIONALLY.
EXAMPLE: CJS (CONDITIONAL JUMP-TO-SUBROUTINE) WITH CONDITION CODE SET AT 'TRUE' BECOMES A JUMP-TO-SUBROUTINE INSTRUCTION. IF THE POLARITY BIT IS SET TO 'INVERT', THIS INPUT IS A 'FALSE' INPUT, CAUSING ALL CONDITIONAL SEQUENCES TO FAIL.

SEE AMD 2904 DESCRIPTION: STATUS AND SHIFT CONTROL UNIT (PAG

DISCNAME: X
FILENAME: STORE.DOC
UPDATED: 24-NOV-80

CONTROL STORE GROUPS - ALU INPUTS

THE ARITHMETIC LOGIC UNITS WITH REGISTER FILE, ARE SIXTEEN BIT UNITS WITH TWO INPUTS (SOURCES), AND ONE OUTPUT (DESTINATION). THE TWO INPUTS ARE IDENTIFIED AS THE 'A' OR LEFT-HAND INPUT, AND THE 'B' OR RIGHT-HAND INPUT; EACH OF SIXTEEN BIT WIDTH. THE A OR B INPUT MAY HAVE AS ITS INPUT SOURCE:

1) ONE OF THE SIXTEEN EXTERNAL REGISTER INPUTS.
2) ONE OF THE SIXTEEN INTERNAL REGISTERS, SELECTED FROM THE REGISTER FILE.

ALU

THE B INPUT HAS HAS THE ADDITIONAL PROPERTIES OF BEING ABLE TO ALTERNATIVELY ACCEPT AS AN INPUT THE CONTENTS OF THE Q- OR TEMPORARY REGISTER. THE B INPUT SELECTION ALSO SPECIFIES WHICH REGISTER WILL BE WRITTEN TO, WITH THE ALU OUTPUT AT THE END OF THE CURRENT MICRO-INSTRUCTION. THESE ADDITIONAL USES OF THE B INPUT, ARE DIRECTED BY INSTRUCTION BITS 10, AND 15 TO 18. THEY WILL BE EXAMINED AFTER REVIEWING THE INPUT SELECTION GROUPS. REGISTERS 0 THROUGH 15 CONSTITUTE THE 'INTERNAL' ALU REGISTER FILE, WHILE OTHER INPUT ARE CONSIDERED 'EXTERNAL.' THE REGISTER FILE IS COMPOSED OF SIXTEEN 16 BIT REGISTERS, WHICH CAN BE USED FOR TEMPORARY PARAMETER STORAGE, OR TO HOLD CONSTANTS FOR CALCULATIONS.

THE EXTERNALLY SELECTED INPUTS ARE:
C-ADDRESS INPUT (FROM THE C-ADDRESS UNIT CONNECTED TO THE C BUS)
D-ADDRESS INPUT (FROM THE D-ADDRESS UNIT CONNECTED TO THE D BUS)
BY PERFORMING ARITHMETIC OPERATIONS ON THIS ADDRESS UNIT AND SETTING THE ADDRESS UNIT GROUP TO 'LOAD,' ADDITION OF CONSTANTS AND BIT SETTING MAY BE DONE IN ONE MICRO-INSTRUCTION.

OUTPUT SELECT CONTROL GROUP

THIS IS A DESCRIPTION OF THE OUTPUT SELECT GROUP OF A CONTROL STORE WORD, IT'S ASSIGNMENT AND USAGE.

THE OUTPUT SELECT GROUP DETERMINES THE 'DESTINATION' REGISTER FOR AN ALU OPERATION. EACH ALU OPERATION CAN INVOLVE TWO SOURCE OPERANDS AND SIX DESTINATION OPERANDS.

THREE OF THESE DESTINATIONS ARE:

- THE Q REGISTER
- AN INTERNAL REGISTER
- AN EXTERNAL REGISTER

THESE ARE SELECTED BY ALU RELATED CONTROL GROUPS.

THE OTHER THREE:

- THE C-ADDRESS
- THE D-ADDRESS
- RANDOM REGISTERS

THESE MAY ALSO BE USED AS AN ALU DESTINATION REGISTER, WHICH WILL BE DECIDED THROUGH THEIR OWN PIPELINE BITS.

WHEN AN 'INTERNAL' REGISTER IS DESIRED AS A DESTINATION, IT IS SELECTED BY THE ALU B INPUT SELECT FIELD, IN CONJUNCTION WITH THE ALU INSTRUCTION FIELD.

WHEN THE Q REGISTER IS DESIRED AS A DESTINATION, IT IS SELECTED THROUGH USE OF THE ALU INSTRUCTION FIELD.

WHEN AN 'EXTERNAL' REGISTER IS DESTINED TO RECEIVE THE ALU OUTPUT WORD, THIS FIELD SELECTS WHICH ONE GETS IT. THE FOLLOWING TABLE INDICATES WHICH NUMBERS SELECT EACH OF THE EXTERNAL REGISTERS.

NOTE: ONLY ONE 'EXTERNAL' REGISTER MAY BE WRITTEN TO DURING A SINGLE MICRO-INSTRUCTION. SELECTING UNUSED OUTPUTS CAUSES NO ILL EFFECTS, AND IT IS RECOMMENDED THAT #0 BE USED AS A DEFAULT WHEN NOT WRITING TO AN EXTERNAL REGISTER.

THE ALU INPUT GROUPS SELECT THE FOLLOWING INPUTS:

EXT/INT	SEL. 3	SEL. 2	SEL. 1	SEL. 0	A INPUT	B INPUT
WHEN BIT 4 IS LOW THE SIXTEEN REGISTERS TAKE EFFECT:						
0	0	0	0	0	0H REGISTER 0	00000 REGISTER 0
0	0	0	0	1	1H REGISTER 1	00001 REGISTER 1
0	0	0	1	0	2H REGISTER 2	00010 REGISTER 2
0	0	0	1	1	3H REGISTER 3	00011 REGISTER 3
0	0	1	0	0	4H REGISTER 4	00100 REGISTER 4
0	0	1	0	1	5H REGISTER 5	00101 REGISTER 5
0	0	1	1	0	6H REGISTER 6	00110 REGISTER 6
0	0	1	1	1	7H REGISTER 7	00111 REGISTER 7
0	1	0	0	0	8H REGISTER 8	01000 REGISTER 8
0	1	0	0	1	9H REGISTER 9	01001 REGISTER 9
0	1	0	1	0	AH REGISTER 10	01010 REGISTER 10
0	1	0	1	1	BH REGISTER 11	01011 REGISTER 11
0	1	1	0	0	CH REGISTER 12	01100 REGISTER 12
0	1	1	0	1	DH REGISTER 13	01101 REGISTER 13
0	1	1	1	0	EH REGISTER 14	01110 REGISTER 14
0	1	1	1	1	FH REGISTER 15	01111 REGISTER 15
1	0	0	0	0	UNUSED	
1	0	0	0	1	UNUSED	
1	0	0	1	0	UNUSED	
1	0	0	1	1	UNUSED	
1	0	1	0	0	UNUSED	
1	0	1	0	1	UNUSED	
1	0	1	1	0	UNUSED	
1	0	1	1	1	UNUSED	

A INPUT		B INPUT		OUTPUT SELECT
011000	UNUSED			
011001	UNUSED			
011010	UNUSED			
011011	UNUSED			
011100	UNUSED			
011101	UNUSED			
011110	UNUSED			
011111	UNUSED			
100000	20H EMIT	10000	10H EMIT	0 NULL
100001	21H C-DATA	10001	11H C-DATA	1 C-DATA
100010	22H C-ADDRESS	10010	12H C-ADDRESS	2 UNUSED
100011	23H D-DATA	10011	13H D-DATA	3 D-DATA
100100	24H D-ADDRESS	10100	14H D-ADDRESS	4 UNUSED
100101	25H RANDOM NUMBER	10101	15H RANDOM NUM.	5 UNUSED
100110	26H UNUSED	10110	16H UNUSED	6 UNUSED
100111	27H C-INPUT BUS	10111	17H C-INPUT BUS	7 UNUSED
101000	28H UNUSED	11000	18H UNUSED	8 UNUSED
101001	29H UNUSED	11001	19H UNUSED	9 UNUSED
101010	2AH UNUSED	11010	1AH UNUSED	A UNUSED
101011	2BH UNUSED	11011	1BH UNUSED	B UNUSED
101100	2CH UNUSED	11100	1CH UNUSED	C UNUSED
101101	2DH UNUSED	11101	1DH UNUSED	D UNUSED
101110	2EH UNUSED	11110	1EH UNUSED	E UNUSED
101111	2FH PRESELECTED A-BUFFER INPUT	11111	1FH PRESELECTED B-BUF. INPUT	F UNUSED
110000	30H PRESELECT A			10 PRESELECT A
110001	31H PRESELECT B			11 PRESELECT B
110010	32H POSTFORMAT			12 POSTFORMAT
110011	33H RANDOM COARSE FEEDBACK			13 RNDM COARSE F-
110100	34H RANDOM FINE FEEDBACK			14 RNDM F
110101	35H MULTIPLY MODE			15 MULTIPLY MODE
110110	36H L. S. PRODUCT READ			16 MULTIPLY X INP
110111	37H M. S. PRODUCT READ			17 MULTIPLY Y INP
111000	38H EXTENDED PRODUCT READ			18 UNUSED
111001	39H LSI-11 OUT			19 UNUSED
111010	3AH LSI-11 IN			1A LSI-11 IN
111011	3BH C-D-BUS/BUFFER REQUEST			1B C,D BUS/BUF. R
111100	3CH C-D-BUS/BUFFER GRANT			1C UNUSED
111101	3DH HORIZONTAL PIXEL COUNT			1D UNUSED
111110	3EH VERTICAL LINE COUNT			1E UNUSED
111111	3FH ALU STATUS			1F UNUSED

ALU A INPUT REGISTERS

#0	REGISTER 0	(REG)	ALU/SEQ
#1	REGISTER 1	(REG)	ALU/SEQ
#2	REGISTER 2	(REG)	ALU/SEQ
#3	REGISTER 3	(REG)	ALU/SEQ
#4	REGISTER 4	(REG)	ALU/SEQ
#5	REGISTER 5	(REG)	ALU/SEQ
#6	REGISTER 6	(REG)	ALU/SEQ
#7	REGISTER 7	(REG)	ALU/SEQ
#8	REGISTER 8	(REG)	ALU/SEQ
#9	REGISTER 9	(REG)	ALU/SEQ
#10	REGISTER 10	(REG)	ALU/SEQ
#11	REGISTER 11	(REG)	ALU/SEQ
#12	REGISTER 12	(REG)	ALU/SEQ
#13	REGISTER 13	(REG)	ALU/SEQ
#14	REGISTER 14	(REG)	ALU/SEQ
#15	REGISTER 15	(REG)	ALU/SEQ
#16	UNUSED		
#17	UNUSED		
#18	UNUSED		
#19	UNUSED		
#20	UNUSED		
#21	UNUSED		
#22	UNUSED		
#23	UNUSED		
#24	UNUSED		
#25	UNUSED		
#26	UNUSED		
#27	UNUSED		
#28	UNUSED		
#29	UNUSED		
#30	UNUSED		
#31	UNUSED		
#32	EMIT		
#33	C-DATA	(REG)	ALU/SEQ
#34	C-ADDRESS	(REG)	ALU/SEQ
#35	D-DATA	(REG)	ALU/SEQ BOARD
#36	D-ADDRESS	(REG)	ALU/SEQ BOARD
#37	RANDOM	(REG)	SELECTOR BOARD
#38	UNUSED		
#39	C-INPUT BUS	(BUS)	
#40	UNUSED		
#41	UNUSED		
#42	UNUSED		
#43	UNUSED		
#45	UNUSED		
#46	UNUSED		
#47	UNUSED		
#48	PRESELECTED INPUTS	B-BUFFER (BUFFER SELECTOR)	BUFFER BOARD (ROUTED THROUGH SELECTOR BOARD)

E A

ALU B INPUT REGISTER

#16	EMIT		
#17	C-DATA	(REG)	ALU/SEQ
#18	C-ADDRESS	(REG)	ALU/SEQ
#19	D-DATA	(REG)	ALU/SEQ BOARD
#20	D-ADDRESS	(REG)	ALU/SEQ BOARD
#21	RANDOM	(REG)	SELECTOR BOARD
#22	UNUSED		
#23	C-INPUT BUS	(BUS)	
#24	UNUSED		
#25	UNUSED		
#26	UNUSED		
#27	UNUSED		
#28	UNUSED		
#29	UNUSED		
#30	UNUSED		
#31	PRESELCTED B-BUFFER INPUTS (BUFFER SELECTOR)		BUFFER BOARD (ROUTED THROUGH SELECTOR BOARD)

BOARD LOCATIONS REGISTERS - OUTPUT SELECTED

THESE REGISTERS ARE CONSIDERED 'WRITABLE' REGISTERS FROM THE OUTPUT OF THE ALU UNIT. THEY ARE STROBED ONE AT A TIME WHEN SELECTED, AT THE END OF A CURRENT MICRO-INSTRUCTION.

ALU EXTERNAL REGISTER

	OUTPUT:	BOARD:	
#0	NULL		
#1	C-DATA	(REG)	ALU/SEQ BOARD
#2	UNUSED		
#3	D-DATA	(REG)	ALU/SEQ BOARD
#4	UNUSED	C-DATA LOW BYTE	
#5	UNUSED	" HIGH "	
#6	UNUSED	D- " LOW "	
#7	UNUSED	" " HIGH "	
#8	UNUSED	NOT DECODED	
#9	UNUSED		
#10	UNUSED		
#11	UNUSED		
#12	UNUSED		
#13	UNUSED		
#14	UNUSED		
#15	UNUSED		
#16	PRESELECT A	(REG)	SELECTOR BOARD
#17	PRESELECT B	(REG)	SELECTOR BOARD
#18	POSTFORMAT	(REG)	ALU/SEQ BOARD
#19	RANDOM COARSE FEEDBACK	(REG)	SELECTOR BOARD
#20	RANDOM FINE FEEDBACK	(REG)	SELECTOR BOARD
#21	MULTIPLY MODE	(REG)	SELECTOR BOARD
#22	MULTIPLY X INPUT	(REG)	SELECTOR BOARD
#23	MULTIPLY Y INPUT	(REG)	SELECTOR BOARD
#24	UNUSED		
#25	UNUSED		
#26	LSI-11 IN	(REG)	
#27	C-D-BUS BUFFER REQUEST	(REG)	
#28	UNUSED		
#29	UNUSED		
#30	UNUSED		
#31	UNUSED		

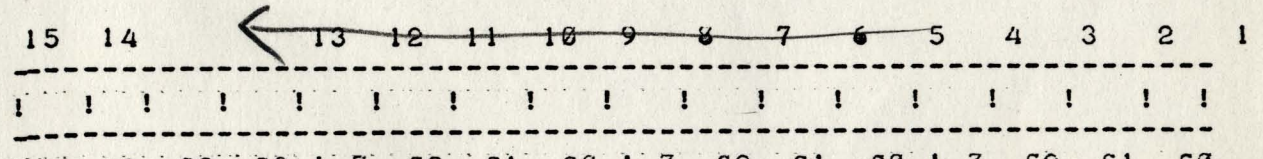
DISCNAME: 0
FILENAME: PRESEL
UPDATED: 18-OCT-79

P R E - S E L E C T R E G I S T E R

THE PRESELECT REGISTER IS USED FOR INPUTTING DATA FROM THE IMAGE BUFFER TO THE ALU UNIT. IT ACTS IN CONJUNCTION WITH THE ALU 'A-(OR B-) INPUT SELECT' BITS IN THE PIPELINE REGISTER. WHEN THE INPUT SELECT BITS ARE SET TO 'PRESELECTED BUFFER INPUTS,' THIS REGISTER'S VALUE DETERMINES WHICH BUFFERS ARE TO BE READ INTO THE ALU INPUT. IT IS A FORM OF FINER SELECTION, DEVELOPED TO IMPLEMENT BUFFER-INDEPENDENT MICRO SUBROUTINES. THESE MICRO SUBROUTINES PERFORM ALGORITHMS WRITTEN WITHOUT REGARD TO THE PARTICULAR BUFFER INVOLVED IN THE OPERATION. THE BUFFER(S) MAY BE 'HOOKED' ONTO THIS MICROPROGRAM THROUGH USE OF THE PRESELECT, POST-FORMAT AND REQUEST REGISTERS, WHILE THE ACTUAL OPERATION IS PERFORMED UPON THE C- OR D-BUS AND THE PRE-SELECTED INPUT(S).

PRESEL

THE PRESELECT A- OR B- REGISTERS ARE FORMATTED AS:



ALU BUFFER PRESELECT INPUT GROUPS (NIBBLES):

15 - 12	11 - 8	7 - 4	3 - 0

TABLE 4:

ZERO	S2	S1	S0	
1	X	X	X	'ZERO' (0000)
0	0	0	0	BUFFER 0
0	0	0	1	BUFFER 1
0	0	1	0	BUFFER 2
0	0	1	1	BUFFER 3
0	1	0	0	BUFFER 4
0	1	0	1	BUFFER 5
0	1	1	0	BUFFER 6
0	1	1	1	BUFFER 7

OPERATION:

THERE ARE TWO PRESELECT REGISTERS, ONE FOR THE A- AND ONE FOR THE B-INPUT TO THE ALU UNIT. EACH IS LOADED THROUGH AN ALU OPERATION, AT LEAST ONE MICROINSTRUCTION BEFORE ITS INTENDED USE.

THE PRESELECT REGISTERS ARE PROGRAMMED BY PLACING THE APPROPRIATE BIT PATTERNS (SEE TABLE 4) INTO THE FOUR INPUT POSITIONS (BY 4 BITS) OF A SIXTEEN BIT ALU INPUT WORD. A SPECIAL PROVISION IS INCLUDED, TO 'MASK OUT' OR FILL WITH ZEROS UNUSED GROUPS OF FOUR BITS, WHEN INPUTTING A BUFFER. THIS CAN BE HANDY WHEN ARITHMETIC OPERATIONS ARE CALCULATED, WHERE THE 'CARRY OUT' OF THE FOUR BIT GROUP IS ENCOUNTERED.

BY PROPER SETTINGS IN THE PRESELECT AND POSTFORMAT REGISTERS, MULTIPLE BUFFER COPY OPERATIONS MAY BE EXECUTED IN THE SAME AMOUNT OF TIME AS A SINGLE BUFFER COPY OPERATION.

SAMPLE:

DISCNAME: 0
FILENAME: POST
UPDATED: 21-NOV-80

P O S T - F O R M A T R E G I S T E R

THIS REGISTER IS USED FOR REPOSITIONING OR 'FORMATTING' THE OUTPUT OF THE ALU OUTPUT BITS. THE NORMAL ASCENDING ORDER OF BIT (ZERO TO FIFTEEN), ARE RE-ROUTED IN FOUR BIT 'NIBBLES' TO MAKE UP A 'POST-FORMATTED' OUTPUT. IT IS AN ALTERNATIVE TO THE SHIFT-AND-ROTATE OPERATIONS BY THE ALU, FOR REPOSITIONING OUTPUTS. IT MAKES POSSIBLE THE SWAP-BYTE OPERATION IN A SINGLE MICROINSTRUCTION, INDEPENDENT OF THE ALU OPERATION. THIS POST-FORMATTING REGISTER ONLY HAS EFFECT UPON THE 'EXTERNAL' REGISTERS (DOES NOT AFFECT THE REGISTER FILE OR THE Q-REGISTER), DUE TO ITS PLACEMENT AT THE ALU OUTPUT.

POSTF

THIS REGISTER IS ORGANIZED AS FOLLOWS:

7	6	5	4	3	2	1	0
S1	S0	S1	S0	S1	S0	S1	S0

POST-FORMATTED OUTPUT BIT GROUPS (NIBBLES):

15-12	11-8	7-4	3-0
BUFFER 3 AND 7	BUFFER 2 AND 6	BUFFER 1 AND 5	BUFFER 0 AND 4

TABLE 5:

S1	S0	
0	0	ALU LOW BITS 0-3
0	1	ALU MIDLOW BITS 4-7
1	0	ALU MIDHIGH BITS 8-11
1	1	ALU HIGH BITS 12-15

THE REGISTER IS LOADED THROUGH AN ALU OPERATION AND WHEN ENABLED, RE-ROUTES THE ALU OUTPUT BITS IN FOUR BIT GROUPS (NIBBLES), TO FORM A NEW SIXTEEN BIT OUTPUT. THE RE-ROUTING IS SELECTED BY PLACING THE ALU OUTPUTS BITS (TABLE 5), INTO THE DESIRED OUTPUT BIT POSITIONS. THE REGISTER MUST BE LOADED (AT LEAST) ONE MICRO-INSTRUCTION PRIOR TO ITS USAGE. IT IS MAINLY USED FOR ALIGNING THE ALU OUTPUT, BEFORE SENDING IT ALONG FOR INPUT TO THE IMAGE BUFFERS. THE FOLLOWING ARE SOME EXAMPLES OF THE POSTFORMAT REGISTER:

1) SWAP BYTE OPERATION:

ALU OUTPUT = 2345 HEXADECIMAL
DESIRED OUTPUT = 4523 HEX

POST-FORMAT REGISTER WOULD BE SET TO 01001110 BINARY = 4E HEX

2) OUTPUT FOUR REPITITIONS OF THE LEAST SIGNIFICANT BITS 0-3:

ALU OUTPUT = 5E37 HEX
DESIRED OUTPUT = 7777 HEX

POST-FORMAT REGISTER WOULD BE SET TO 00000000 BINARY = 00 HEX

ARITHMETIC/LOGIC UNIT OUTPUT BITS:

15 - 12	11 - 8	7 - 4	3 - 0

POST-FORMATTED OUTPUT BITS:

15 - 12	11 - 8	7 - 4	3 - 0

ANY NIBBLE (OF FOUR BITS) OF THE ALU OUTPUT MAY BE RE-ROUTED TO ANY NIBBLE OF THE POST FORMATTED OUTPUT.

FIGURE 5:

DISCNAME: 0
FILENAME: ADUNIT
UPDATED: 31-JUL-79

SWITCH PER SECOND

ADDRESS UNIT CONTROL GROUPS

THE ADDRESS UNITS CONSIST OF 16 BIT UP/DOWN COUNTERS. THEY HAVE FIVE MAJOR MODES OF OPERATION. THESE ARE:

1) CLEAR CURRENT ADDRESS TO ZERO
2) INCREMENT ADDRESS BY ONE (COUNT UP)
3) DECREMENT ADDRESS BY ONE (COUNT DOWN)
4) LOAD IN A VALUE PRESENT AT THE ALU OUTPUT
5) HOLD - DO NOTHING - HOLD PRESENT ADDRESS

THE C-ADDRESS USES P61-P64, THE D-ADDRESS P65-68. THESE FIVE MODES ARE ACTIVATED BY THESE BIT PATTERNS IN THE ADDRESS UNIT CONTROL GROUPS:

(MSB) ENABLE/ HOLD	LOAD/ COUNT	UP/ DOWN	CLEAR (LSB)	
1	X	X	1	CLEAR
1	0	1	0	INCREMENT
1	0	0	0	DECREMENT
1	1	X	0	LOAD
0	X	X	X	HOLD

C-D-BUS ADDRESS CONTROL UNITS

A ONE IS A HIGH, A ZERO IS A LOW, AND AN 'X' IS A DON'T CARE CONDITION.

EACH ADDRESS UNIT MAY BE CONTROLLED INDEPENDENTLY OF THE OTHER, AND MAY TAKE IN THE SAME ALU OUTPUT DURING THE LOAD OPERATION. ALL OPERATIONS OF THE ADDRESS UNIT TAKE EFFECT AT THE END OF THE CURRENT MICROINSTRUCTION. THE ALU OUTPUT IS ALSO AVAILABLE AT THE END OF THE CURRENT MICROINSTRUCTION, ENABLING ARITHMETIC/LOGICAL OPERATIONS TO BE PERFORMED IN ONE MICRO-CYCLE, UPON THE CONTENTS THE ADDRESS REGISTER. THIS IS USED TO CALCULATE VERTICALLY RELATED OFFSETS, AND MORE COMPLEX ADDRESSING SCHEMES WHEN INCREMENTING OR DECREMENTING ARE INAPPROPRIATE. ADDITION OF A VERTICAL OFFSET (128 PIXELS) MAY BE ACCOMODATED BY THESE STEPS:

PLACE THE 'EMIT' GROUP A 128 DECIMAL
THE ALU A INPUT AT 'EMIT'
THE ALU B INPUT AT C-ADDRESS (OR D-ADDRESS)
C-ADDRESS UNIT TO LOAD
THE ALU INSTRUCTION TO A PLUS B

THE CURRENT VALUE OF C-ADDRESS UNIT WILL BE ADDED TO THE VALUE OF THE EMIT GROUP (128 DECIMAL), AND THEN RELOADED INTO C-ADDRESS UNIT. THIS ADDITION ADDRESSES THE PIXEL JUST BELOW THE PREVIOUS ONE.

DISCNAME: 0
FILENAME: BUSCON
UPDATED: 31-JUL-79

C - A N D D - B U S C O N T R O L G R O U P S

THE BUS CONTROL GROUPS CONNECT TO THE C AND D BUSES OF THE BUFFER MEMORIES. THESE CONTROL LINES ARE TAPPED DIRECTLY OFF THE PIPLINE REGISTER, AND SENT TO THE BUFFER READ/WRITE (L) AND THE BUFFER ENABLE(L) LINE FOR EACH OF THESE TWO BUSES. THEY DETERMINE THE MODE OF THE BUFFER, WHEN THE BUFFER IS CONNECTED TO THAT CONTROL BUS. THESE CONTROL BITS TAKE EFFECT AT THE BEGINNING OF THE MICROINSTRUCTION, AND LAST FOR THE DURATION OF THE INSTRUCTION CYCLE. THE D-BUS IS USED ONLY FOR BUFFER OPERATIONS. THE D-BUS CONTROL BITS SET UP THREE MODES:

1) READ CYCLE:
   THE BUFFER CONNECTED TO THE C OR D BUS ACCESSES THE LOCATION IN THE RESPECTIVE ADDRESS UNIT. THE OUTPUT IS AVAILABLE AT THE END OF THE MICROCYCLE, AND IS LATCHED AT THE OUTPUT OF THE BUFFER.
2) WRITE CYCLE:
   BUFFERS CONNECTED TO THE CONTROL BUS PERFORM A WRITE CYCLE. DATA PRESENT ON THE DATA INPUT BUS IS WRITTEN INTO THE LOCATION PRESENT ON THE ADDRESS BUS. THE DATA PRESENT AT THE BEGINNING OF THE MICROINSTRUCTION TAKES EFFECT FOR THE DURATION OF THE MICROCYCLE. THE LOOPED-AROUND DATA IS AVAILABLE AT THE BUFFER OUTPUT AT THE END OF THE CYCLE.
3) DISABLE:
   THE BUFFER IS PLACED INTO A DISABLED STATE. THE OUTPUT OF THE PREVIOUS CYCLE IS HELD DURING A BUFFER DISABLE. READ OR WRITE CYCLES ARE NOT PERFORMED WHILE THIS BUS IS CONNECTED TO THE BUFFER, BUT THE BUFFER CONTENTS REMAIN UNCHANGED (STORED DATA IS NOT LOST).

D-BUS CONTROL USE PIPELINE BITS P73, P74. THESE THREE MODES ARE ACTIVATED WITH THE FOLLOWING BIT PATTERNS IN THE CONTROL GROUP:

READ/ WRITE(L)	ENABLE(L)	
X	1	DISABLE
0	0	WRITE
1	0	READ

RELOCATE

DISCNAME: 0
FILENAME: PIXREG
ENTERED: 4-AUG-79

PIXEL PROCESSOR REGISTER

REGISTER A-IN 3F HEX

BIT 0 - CARRY
BIT 1 - OVERFLOW
BIT 2 - ZERO STATUS
BIT 3 - NEGATIVE
BIT 4 - SHIFT IN/OUT LSB
BIT 5 - Q REGISTER SHIFT IN/OUT LSB
BIT 6 - SHIFT IN/OUT MSB
BIT 7 - Q REGISTER SHIFT IN/OUT MSB
BIT 8 - 15 UNUSED

DISCNAME: C
FILENAME: CBUS
UPDATED: 24-NOV-80

THE 'C' BUS CONTROL BITS

THE C-BUS CONNECTS AND INTERFACES TO SOME GENERAL PURPOSE ELEMENTS, LIKE THE 4K BY 16 BITS READ/WRITE SCRATCH-PAD MEMORY. ITS STRUCTURE:

1) A 16 BIT ADDRESS BUS, DRIVEN BY THE C-ADDRESS REGISTER.
2) A 16 BIT DATA OUTPUT, DRIVEN BY THE C-DATA REGISTER.
3) A 16 BIT DATA INPUT BUS, ENTERING THE ALU INPUT SELECTORS, A AND B INPUTS.
4) A 4 BIT CONTROL BUS, FOR MANIPULATING DATA FLOW ON THE DATA AND ADDRESS LINES DRIVEN BY THE ALU/SEQUENCER PIPELINE REGISTER.

THE CONTROL BUS IS DEFINED AS FOLLOWS:

C-BUS ENABLE(L)	C-BUFFER ENABLE(L)	BUFFER READ/ WRITE(L)	C-BUS WRITE(L) C-BUS READ(L)
1 BIT P69	1 BIT P70	1 BIT P71	1 BIT P72 (MSB)

TABLE:

C-BUS READ(L) P72	BUF.R/W P71	BUFFER BUS W(L) P70	C-BUS EN(L) P69		EN(L) FUNCTION:
0	0	0	0	0	C-BUS READ, C-BUS WRIT, BUF. WRIT
0	0	0	1	1	BUFFER WRITE
0	0	1	0	2	C-BUS READ
0	0	1	1	3	DISABLE
0	1	0	0	4	C-BUS R, C-BUS W, BUFFER WRITE
0	1	0	1	5	BUFFER READ
0	1	1	0	6	C-BUS READ
0	1	1	1	7	DISABLE
1	0	0	0	8	C-BUS WRITE, BUFFER WRITE
1	0	0	1	9	BUFFER WRITE
1	0	1	0	A	C-BUS WRITE
1	0	1	1	B	DISABLE
1	1	0	0	C	BUFFER READ
1	1	0	1	D	BUFFER READ
1	1	1	0	E	DISABLE
1	1	1	1	F	DISABLE (DEFAULT)

RESERVATION: ROWS 1,2,3, AND 5 ARE PRONE TO ERRONEOUS RESULTS.

THE OPERATION OF THE BUS CAN BE EXPLAINED BY EXAMINING THE READ AND WRITE BUS CYCLES AS EXAMPLES OF THE BUS'S OPERATION:

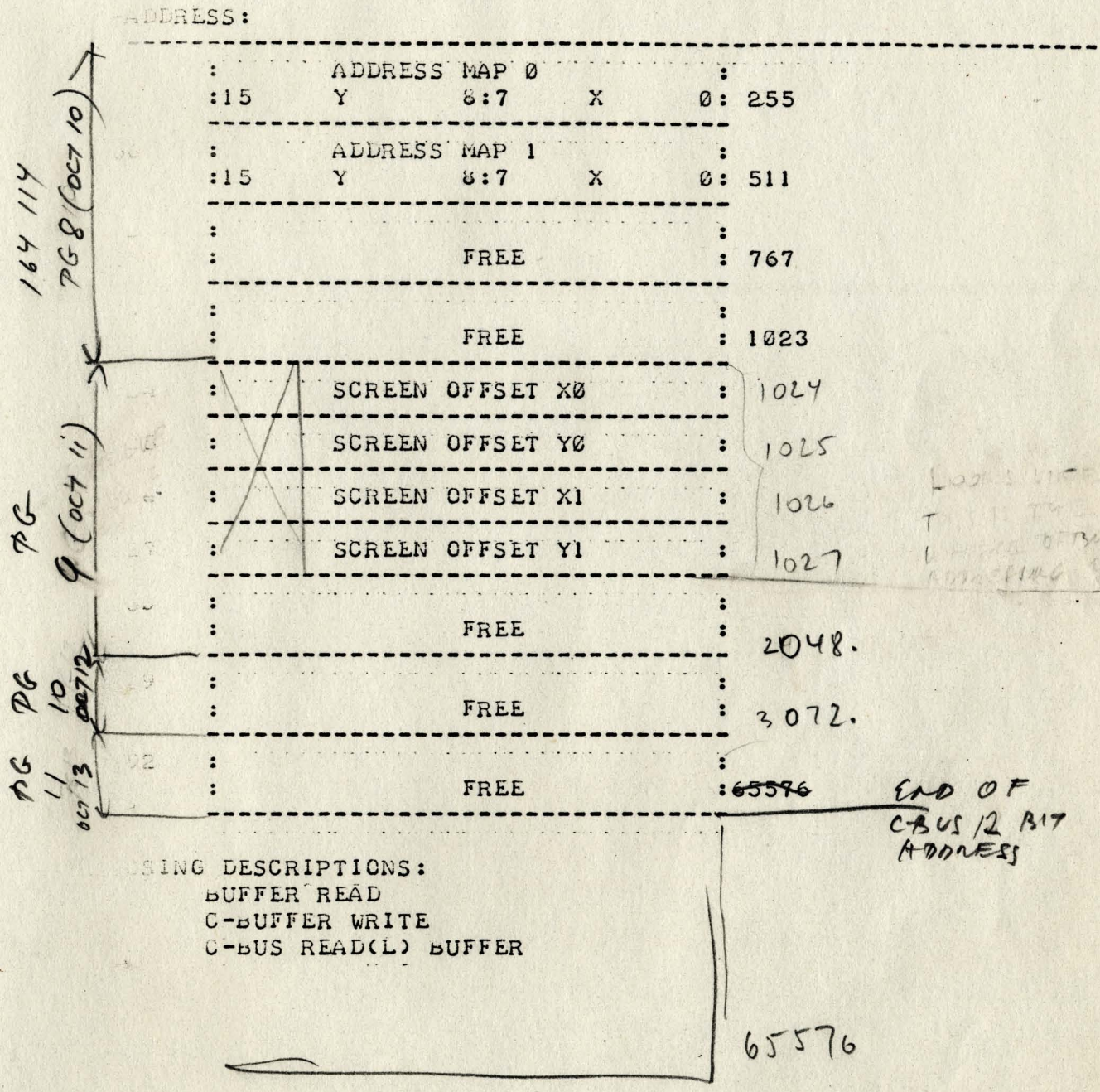
READ CYCLE:

1) SETUP THE DESIRED MEMORY ADDRESS BY PLACING IT IN THE C-ADDRESS REGISTER, THROUGH AN ALU OPERATION.
2) IN THE PIPELINE REGISTER: PLACE BUS ENABLE(L) AT LOW, INDICATING A BUS OPERATION, AND C-BUS READ(L) AT LOW, INDICATING A READ CYCLE.
3) WAIT FOR MEMORY ACCESS.
4) TAKE IN THE ACCESSED DATA THROUGH THE C DATA INPUT BUS THROUGH THE A OR B INPUT SELECTORS OF THE ALU.
5) IN THE PIPELINE REGISTER: PLACE 'BUS ENABLE(L)' AND C-BUS READ(L) AT A HIGH LEVEL, MARKING THE END OF THE CURRENT BUS CYCLE.

WRITE CYCLE:

1) SET UP THE DESIRED MEMORY ADDRESS, IN THE C-ADDRESS REGISTER, THROUGH AN ALU OPERATION.
2) SET UP DESIRED DATA TO BE WRITTEN IN THE C-DATA REGISTER.
3) IN THE PIPELINE REGISTER: PLACE BOTH BUS ENABLE(L) AND THE C-BUS WRITE(L) BITS AT A LOW, INDICATING A BUS WRITE CYCLE.
4) WAIT FOR THE WRITE CYCLE'S COMPLETION.
5) IN THE PIPELINE REGISTER: PLACE BUS ENABLE BIT AT A HIGH LEVEL AND THE C-BUS WRITE BIT HIGH, ENDING THE CURRENT BUS CYCLE.

C-BUS ADDRESS MAP



DISCNAME: 0
FILENAME: RGRANT
UPDATED: 24-NOV-80

R E Q U E S T - G R A N T R E G I S T E R S

THE REQUEST REGISTER IS USED BY THE VIDEO PROCESSOR, TO REQUEST USAGE OF ONE OR MORE IMAGE BUFFERS, ON THE C- OR D-BUS. IF THE REQUEST IS OF THE HIGHEST PRIORITY THE BUFFER WILL CONNECT ITSELF TO THE DESIRED BUS, WITHIN ONE BUFFER CYCLE. THE CONNECTING IS HANDLED BY THE PRIORITY LOGIC ASSOCIATED WITH EACH BUFFER. THIS CONNECTION MAY BE VERIFIED BY THE VIDEO PROCESSOR BY COMPARING THE CONTENTS OF THE REQUEST REGISTER TO THE GRANT REGISTER. IF THEY ARE IDENTICAL, ALL REQUESTS WILL BE GRANTED, AND THE BUFFERS WILL BE CONNECTED TO THE REQUESTED BUS(ES). A TEST BIT, AVAILABLE TO THE SEQUENCER CALLED THE REQUEST=GRANT BIT, IS LOW WHEN THE REQUEST REGISTER IS EQUAL IN CONTENT TO THE GRANT REGISTER, AND HIGH OTHERWISE. IT IS A CONVENIENT WAY OF ACTIVATING SUBPROGRAMS UPON CONNECTION OF THE BUFFER(S), BY USING CONDITIONAL SEQUENCING OF THE MICROPROGRAM.

BUF-REQ-GRAN

THE REQUEST REGISTER, A-IN = 3B HEX:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
BUFFERS 7-0, D BUS REQUESTS								BUFFERS 7-0, C BUS REQUESTS							

REQUESTED = ~~1 (ONE)~~ 0 ZERO, NOT REQUESTED = ~~0 (ZERO)~~ 1 ONE

THE GRANT REGISTER: A-IN = 3C HEX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
BUFFERS 7-0, D BUS REQUESTS								BUFFERS 7-0, C BUS REQUESTS							

REQUESTED = ~~1 (ONE)~~ 0 ZERO, NOT REQUESTED = ~~0 (ZERO)~~ 1 ONE

WHEN SET, THESE BITS REQUEST CONNECTION OF AN IMAGE BUFFER TO C- OR D- BUSES, ORIGINATING FROM THE VIDEO PROCESSOR. THE GRANT REGISTER INDICATES THE SUCCESS OF THE REQUEST. THE REQUEST BIT MUST BE HELD AT A ONE FOR THE DURATION OF ACCESS TO A BUFFER. IF PLACED AT ZERO, THE BUFFER IS FREE TO CONNECT TO OTHER DEVICES (LSI-11, X-Y GENERATOR, ETC...).

DISCNAME: 0
FILENAME: MULTIP
UPDATED: 24-NOV-80

HIGH SPEED MULTIPLIERS

ADDRESS RE-ASSIGNMENT IS ACHIEVED BY THE USE OF A HIGH SPEED DIGITAL MULTIPLIERS. THE TASK OF SKIPPING PIXELS IS THEN ACCOMODATED THROUGH ROUND-OFF AND TRUNCATION ERROR OF THE MULTIPLIER.

IN SCAN PROCESSING FOUR QUADRANT MULTIPLIERS ARE USED TO AMPLITUDE MODULATE THE DEFLECTION RAMPS, RESULTING IN A MODULATION OF THE DISPLAYED RASTER.

IN BUFFER SCANNING TWO DIGITAL RAMPS ARE USED, ONE FOR THE HORIZONTAL AND ONE FOR THE VERTICAL AXES. THESE RAMPS ARE ROUTED TO THE ADDRESS INPUTS OF THE BUFFER, WHICH TIMES THE INFORMATION CONTENT TO THE VIDEO TIMING (SYNCHRONIZATION) SIGNALS.

MULTI

COMPRESSION AND EXPANSION OF A BUFFERED IMAGE REQUIRES MULTIPLICATION OF THE ADDRESSING RAMPS, FOLLOWED BY A DIGITAL AUTOMATIC GAIN CONTROL. MULTIPLICATION DETERMINES A SLOPE OR RATE OF ADDRESSING THE STORED IMAGE, EXPANDING ITS SIZE BY A SLOWER ADDRESS SCANNING WHILE COMPRESSING IT BY A FASTER ONE. THE AUTOMATIC GAIN CONTROL ASSURES A FULL READ-OUT OF THE ADDRESSED IMAGE SPACE. THE SKIPPING OF PIXELS IS DETERMINED BY MULTIPLICATION, FOLLOWED BY AN AUTOMATIC GAIN CONTROL. OTHER RESTRAINTS SHOULD INCLUDE MULTIPLICATION BY RATIONAL OR FRACTIONAL NUMBERS, TO AVOID GROSS CHANGES IN PICTURE SIZE (1/2 SIZE, 1/3 SIZE, 1/4 SIZE ETC.).

A PSEUDO RANDOM NOISE GENERATOR CAN BE IMPLEMENTED WITH A VARIATION ON A SHIFT REGISTER WITH FEEDBACK, ITS NEXT INPUT DETERMINED BY ADDITION OF CHOSEN BITS OF IT'S OUTPUT. THE SHIFT REGISTER MAY BE LOADED OR CLEARED DURING THE HORIZONTAL OR VERTICAL BLANKING INTERVALS TO ALLOW A "SYNCHRONIZED" OR FRAME LOCKED NOISE SOURCE. BY VARYING THE LENGTH OF THIS SHIFT REGISTER AND ITS FEEDBACK PATHS, DIFFERENT SEQUENCE LENGTHS MAY BE OBTAINED. THE FREE RUNNING MODE, DRIVEN BY AN X/Y CLOCK, WOULD GENERATE AN UNLOCKED NOISE SOURCE CAUSED BY MISMATCHING THE PSEUDO RANDOM NOISE SEQUENCE TO THE VIDEO LINE/FIELD BLANKING RATE. MULTIPLE SHIFT REGISTERS COULD GENERATE LARGER 'NOISE WORDS,' OR THE SHIFT REGISTER'S INSTANTANEOUS PARALLEL OUTPUT COULD BE MAPPED TO GENERATE LARGER WORDS.

HARDWARE MULTIPLIER/ACCUMULATOR UNIT

THE ALU SECTION CONTAINS A HIGH SPEED MULTIPLIER/ACCUMULATOR WHICH IMPLEMENTS 16 BIT BY 16 BIT MULTIPLICATION, AND SUM OF PRODUCT COMPUTATIONS. THESE FUNCTIONS ARE USEFUL FOR CALCULATING INFINITE SERIES, AVERAGE INTENSITY, AND FADING TWO IMAGES ON A PIXEL BY PIXEL BASIS.

THE MULTIPLIER IS ACCESSED THROUGH 'EXTERNAL' REGISTERS AT THE OUTPUT OF THE ALU, WITH RESULTS AVAILABLE ON THE A-INPUT HALF OF THE ALU.

THESE REGISTERS ARE:

1) A 'MODE' REGISTER
   THIS REGISTER SETS THE MULTIPLIER MODE, SELECTING TWO'S COMPLEMENT/MAGNITUDE ONLY, ROUNDED RESULT/TRUNCATED RESULT, AND STRICT MULTIPLICATION/SUM OF PRODUCTS.
2) THE 16 BIT 'X' OPERAND (X-INPUT)
3) THE 16 BIT 'Y' OPERAND (Y-INPUT)
   WHEN SET TO MULTIPLY, THE PRODUCT IS THE RESULT OF MULTIPLICATION OF THE X AND Y INPUTS TO FORM A 32 BIT PRODUCT. THIS PRODUCT IS CONTAINED IN TWO 16 BIT REGISTERS, ACCESSED THROUGH THE A-INPUT SIDE OF THE ALU
4) THE MOST SIGNIFICANT PRODUCT REGISTER (MSP)
   CONTAINING THE UPPER 16 BIT PRODUCT
5) THE LEAST SIGNIFICANT PRODUCT REGISTER (LSP)
   CONTAINING THE THE LOWER 16 BITS OF THE PRODUCT *

   WHEN IN THE ACCUMULATE MODE, THE PRODUCT FORMED IS AVAILABLE TO THREE ACCURACY BITS, ACCESSED THROUGH THE A-INPUT SIDE OF THE ALU:

6) THE EXTENDED PRODUCT REGISTER (XTP)
   CONTAINS THE EXTENDED BITS OF ACCUMULATE OPERATIONS IN ITS LEAST SIGNIFICANT THREE BIT POSITIONS.

* YOU MUST FIRST READ MSP, THEN LSP (TIMING ON LSP LATCH

MULTIPLIER MODE REGISTER

3	2	1	0
ACCUMUL/MULTIPL	SUBSTRACT/ADD	ROUND/TRUNCATE	TWO'S COMPLMNT

THE MULTIPLIER MODE REGISTER IS USED TO SET UP THE OPERATING MODE OF THE HARDWARE MULTIPLIER/ACCUMULATOR. THIS REGISTER IS ACCESSED AS AN 'EXTERNAL' ALU REGISTER AND IS FOUR BITS IN WIDTH. IT MAY ALSO BE READ BACK BY THE ALU THROUGH THE A-INPUT SIDE.

ITS FOUR BITS ARE:

BIT 0 - TWO COMPLEMENT/UNSIGNED MAGNITUDE (L)
THIS BIT WHEN SET PLACES THE MULTIPLIER INTO TWO'S COMPLEMENT MODE. NUMBERS ARE REPRESENTED IN A TWO'S COMPLEMENT SIXTEEN BIT WORD, WITH THE MOST SIGNIFICANT BIT BEING THE SIGN BIT. WHEN IN 'NON-ACCUMULATING MODE' THE SIGN BIT IS CARRIED OVER TO ALL BITS OF THE 'EXTENDED PRODUCT REGISTER', AS WELL AS THE TOP BIT OF THE 'MOST SIGNIFICANT PRODUCT' REGISTER.
WHEN LOW, THE MULTIPLIER IS PLACED IN UNSIGNED MAGNITUDE NOTATION OF SIXTEEN BITS WIDTH.

BIT 1 - ROUND/TRUNCATE (L)
WHEN SET, THE MULTIPLIER 'ROUNDS' THE PRODUCT BY ADDING ONE TO MSB OF THE LEAST-SIGNIFICANT-PRODUCT (LSP) REGISTER. THIS IS EQUIVALENT TO THE ADDITION OF ONE HALF WITH THE 'BINARY POINT' ASSUMED TO BE BETWEEN THE LSP AND MSP REGISTER. WHEN LOW THE MULTIPLIER TRUNCATES (DOES NOT ROUND) THE MOST SIGNIFICANT PRODUCT.

BIT 2 - SUBTRACT/ADD (L)
BIT 2 OPERATES IN CONJUNCTION WITH BIT 3. WHEN BIT 3 IS SET TO 'ACCUMULATE' MODE, THIS BIT DETERMINES WHETHER A 'SUM OF PRODUCTS' (ADD MODE) OR A 'DIFFERENCE OF PRODUCTS' (SUBTRACT MODE) IS FORMED DURING SUCCESSIVE STEPS IN THE ACCUMULATION.
ADD = 0, SUB = 1

BIT 3 - ACCUMULATE/MULTIPLY (L)
THIS BIT SELECTS BETWEEN A SIMPLE PRODUCT (MSP,LSP = X-IN * Y-IN), OR AN ACCUMULATION OF PRODUCTS:
IN ADD MODE: $P(N) = X(N) * Y(N) + P(N-1)$
IN SUB MODE: $P(N-1) - X(N) * Y(N)$

P IS A SUBSCRIPT MULTIPLICATION
N IS THE CURRENT MULTIPLICATION
N-1 IS THE PREVIUOS MULTIPLICATION

P(N) IS READ BACK AS A 35 BIT PRODUCT
LSB = LEAST SIGNIFICANT 16 BITS
MSB = MOST SIGNIFICANT 16 BITS
XTB = EXTRA (ACCURACY) BITS

FOR ADDITIONAL INFORMATION SEE THE TRW SPEC SHEET FOR TDC 1010J

DISCNAME: X
FILENAME: RANDOM.DOC
UPDATED: 21-OCT-79

RANDOM NUMBER GENERATOR

THE PIXEL PROCESSOR CONTAINS A HIGH SPEED RANDOM NUMBER GENERATOR. IT IS ACCESSIBLE FOR MODIFYING THE RANDOM NUMBER SEQUENCE IN LENGTH, SPEED OF GENERATION, AND STARTING VALUE (SEED). IT IS CONSTRUCTED OUT OF A SIXTEEN BIT SHIFT REGISTER WITH AN INPUT DERIVED FROM A SELECTED COMBINATION OF THE CURRENT OUTPUT. THIS SHIFT REGISTER MAY BE LOADED (SEEDED) FROM THE ALU UNIT OF THE PIXEL PROCESSOR. A SINGLE STEP CLOCK STEPS UNDER PROGRAM CONTROL TO THE NEXT NUMBER IN THE SEQUENCE.

THE FEEDBACK PATH IS DERIVED BY SELECTING UP TO FOUR BITS OF THE CURRENT OUTPUT, AND EXCLUSIVE-ORING THEM TO FORM THE INPUT TO THE SHIFT REGISTER. BY CHOOSING APPROPRIATE FEEDBACK PATHS, THE LENGTH OF THE SEQUENCE MAY BE VARIED, WITH THE LEAST SIGNIFICANT BITS OF THE CHOSEN LENGTH BEING THE OUTPUT.

FOR PROPER OPERATION, THE 'SEED' NUMBER MUST NOT BE ALL ZEROS. IF IT WERE, THE SEQUENCE WOULD BE CONTINUOUS ZEROS (NOT THAT RANDOM A PATTERN).

THE LONGEST SEQUENCE POSSIBLE WITH THIS RANDOM NUMBER GENERATOR IS: (2**N)-1 (TWO TO THE NTH POWER MINUS ONE). WITH LENGTH AND SEQUENCE IS DETERMINED BY THE SELECTED FEEDBACK PATTERN CHOSEN. THE SEQUENCE MAY BE SHIFTED FROM ITS STARTING POINT BY LOADING A NEW 'SEED' NOT EQUAL TO ZERO. FOR BUFFER ADDRESSING THE THE 16 BIT SEQUENCE IS LONGER THAN NEEDED IN THE STANDARD 'VERTICAL SPLIT MODE'. THIS MODE NEEDS (2**14)-1 PIXELS, OR 16384(16K). SETTING THE SEQUENCE LENGTH TO 14, GENERATES 16383 OF THESE ADDRESSES, THE MISSING ADDRESS BEING THE UBIQUITOUS ZERO.

RAN

RANDOM NUMBER MODE - PIPELINE CONTROL GROUP

THE RANDOM NUMBER MODE IS CONTROLLED THROUGH TWO BITS OF THE PIPELINE (P75 AND P76). THESE BITS FUNCTION ALONG WITH THE TWO FEEDBACK REGISTERS, TO SPECIFY OPERATION OF THE RANDOM NUMBER GENERATOR. THE BITS ACT AS SHOWN IN TABLE BELOW:

TABLE 1:

PIPE76	PIPE75	
0	0	HOLD
0	1	SHIFT SEQUENCE LEFT
1	0	SHIFT SEQUENCE RIGHT
1	1	LOAD (FROM ALU OUTPUT)

EACH ALU CLOCK WILL RESULT IN ONE EXECUTION OF THESE CONTROL BITS.

EXAMPLE: P76 = 0
P75 = 1
EACH ALU CLOCK ADVANCES THE SEQUENCE BY ONE SHIFT LEFT.

FEEDBACK BIT SELECTION

THE FEEDBACK PATH IS DERIVED FROM THE CURRENT OUTPUT BY USE OF TWO SETS OF SELECTORS: A COARSE SELECTOR, AND A FINE SELECTOR. BOTH ACT TOGETHER AS A SINGLE LARGE SELECTOR TO FORM THE NEXT INPUT TO THE SHIFT REGISTER (THE FEEDBACK BIT).

COARSE FEEDBACK REGISTER

THIS REGISTER IS USED TO SELECT THE FEEDBACK PATH OF THE COARSE SELECTOR. THE COARSE SELECTOR CHOOSES FOUR BITS OF THE CURRENT SIXTEEN BIT RANDOM NUMBER. THESE BITS ARE PASSED ALONG TO FINE SELECTOR FOR EXCLUSIVE-ORING TO FORM THE 'FEEDBACK BIT'. THE FOUR BITS ARE SELECTED, BY PLACING THE APPROPRIATE NUMBER (SEE TABLE 2) INTO THE COARSE-SELECT-REGISTER.
THE REGISTER IS OUTLINED BELOW:

! 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 !
! S3	S2	S1	S0	S3	S2	S1	S0	S3	S2	S1	S0	S3	S2	S1	S0 !
! BIT #3				BIT #2				BIT #1				BIT #0			!

TABLE 2:

HEX.	S3	S2	S1	S0		
0	0	0	0	0	-	BIT 0
1	0	0	0	1	-	BIT 1
2	0	0	1	0	-	BIT 2
3	0	0	1	1	-	BIT 3
4	0	1	0	0	-	BIT 4
5	0	1	0	1	-	BIT 5
6	0	1	1	0	-	BIT 6
7	0	1	1	1	-	BIT 7
8	1	0	0	0	-	BIT 8
9	1	0	0	1	-	BIT 9
A	1	0	1	0	-	BIT 10
B	1	0	1	1	-	BIT 11
C	1	1	0	0	-	BIT 12
D	1	1	0	1	-	BIT 13
E	1	1	1	0	-	BIT 14
F	1	1	1	1	-	BIT 15

FINE FEEDBACK REGISTER

THIS REGISTER FURTHER 'FINE SELECTS' THE COARSE SELECTED BITS (BITS 0, 1, 2 AND 3), FOR INCLUSION IN THE CALCULATION OF THE 'FEEDBACK BIT'. THE FEEDBACK BIT IS DETERMINED BY SELECTIVELY EXCLUSIVE-ORING (ONE BIT ADDITION) THESE BITS:

REGISTER:

BITS 15-4 UNUSED	BIT 3 EN	BIT 2 EN	BIT 1 EN	BIT 0 EN

USE THE BITS IN ASCENDING ORDER (FIRST BIT FIRST, ETC). THE POSITION OF EXOR (+) HOWEVER, IS NOT DEPENDENT ON THE BIT POSITION, OR ON ENTERING OF THE BITS (BIT 1 (+) BIT 2 (+) BIT 4 = BIT 4 (+) BIT 1 (+) BIT 2).

SETTING THE BIT 'ON' INCLUDES IT IN THE FEEDBACK BIT. THE ALL ZERO NUMBER IS NOT NORMALLY USED. FEEDBACK BITS 0, 1, 2 AND 3 REFER TO THE BITS SELECTED BY THE COARSE FEEDBACK REGISTER.

TABLE 3:

BIT 3 EN	BIT 2 EN	BIT 1 EN	BIT 0 EN	RESULTING FEEDBACK BIT (TO RANDOM REGISTER INPUT)
0	0	0	0	'ZERO' (0)
0	0	0	1	BIT 0
0	0	1	0	BIT 1
0	0	1	1	BIT 0 EXOR BIT 1
0	1	0	0	BIT 2
0	1	0	1	BIT 0 EXOR BIT 2
0	1	1	0	BIT 1 EXOR BIT 2
0	1	1	1	BIT 0 EXOR BIT 1 EXOR BIT 2
1	0	0	0	BIT 3
1	0	0	1	BIT 0 EXOR BIT 3
1	0	1	0	BIT 1 EXOR BIT 3
1	0	1	1	BIT 0 EXOR BIT 1 EXOR BIT 3
1	1	0	0	BIT 2 EXOR BIT 3
1	1	0	1	BIT 0 EXOR BIT 2 EXOR BIT 3
1	1	1	0	BIT 1 EXOR BIT 2 EXOR BIT 3
1	1	1	1	BIT 0 EXOR BIT 1 EXOR BIT 2 EXOR BIT 3

PSEUDO RANDOM SEQUENCE LENGTH

# OF BITS N	SEQUENCE LENGTH 2**N-1	'COARSE' FEEDBACK BITS FEEDBACK BITS	
2	3	0,1	
3	7	1,2	
4	15	2,3	
5	31	2,4	
6	63	4,5	
7	127	5,6 [3,6]	
8	255	1,2,4,7 (4,5,6,7)	
9	511	4,8	
10	1,023	6,9	
11	2,047	8,10	
12	4,095	5,7,10,11	(2,8,9,11)
13	8,191	8,9,11,12	(8,10,11,12)
14	16,383	3,7,12,13	
15	32,767	13,14	
16	65,535	3,12,14,15	

THIS TABLE IS FROM ELECTRONOTES 'MUSICAL ENGINEERS HANDBOOK' CHAPTER 5 - SECTION H - PAGE 4
DATA IN () ARE FROM DON LANCASTER TTL COOKBOOK. DATA IN [] ARE ALTERNATIVES.

DISCNAME: X
FILENAME:RITBUF.DOC
UPDATED: 25-JUN-79

WRITING THE IMAGE BUFFERS

THIS IS A STEP BY STEP DESCRIPTION OF HOW TO GET DATA FROM THE VIDEO PIXEL PROCESSOR TO THE IMAGE BUFFERS.

THE IMAGE BUFFERS CONSIST OF EIGHT 8K BY 4 BIT MULTI-PORT MEMORIES, ACCESSIBLE THROUGH FOUR SOURCES.

A BUS: THE LSI-11
B BUS: THE DISPLAY TIMING/REAL TIME DIGITIZED INPUT
C BUS: THE VIDEO PIXEL PROCESSOR
D BUS: THE VIDEO PIXEL PROCESSOR

WRITING FROM THE VIDEO PROCESSOR-C BUS:

DATA MUST BE ROUTED THROUGH THE ALU UNITS TO ARRIVE AT THE IMAGE BUFFERS. THESE ARE THE STEPS NEEDED TO IDENTIFY RELEVANT OPERATIONS.

TO CONNECT THE BUFFER TO THE C BUS:

1) REQUEST THE DESIRED BUFFER THROUGH THE 'C-REQUEST' REGISTER.
2) VERIFY THAT YOU HAVE BEEN 'GRANTED' USAGE OF THE BUFFER BY:
   A) COMPARING THE 'C-REQUEST' REGISTER TO THE 'C-GRANT' REGISTER THROUGH THE ALU. WHEN EQUAL, THE REQUEST HAS BEEN GRANTED AND THE C BUS NOW CONTROLS THE BUFFER.
   B) USING THE C-REQUEST = C-GRANT TEST BIT, AVAILABLE AS A TEST CONDITION INPUT TO THE SEQUENCER. THIS WILL BE ACCURATE ONLY WHEN ALL REQUESTED BUFFERS HAVE BEEN GRANTED.

PROGRAM NOTES

TO WRITE DATA INTO THE BUFFER:

THE C BUS DATA IS 'ALIGNED' INTO 4 BIT 'NIBBLES' IN THE 16 BIT DATA OUTPUT. THIS ALIGNMENT OF OUTPUT BITS IS ORGANIZED BEFORE BEING SENT ALONG TO THE BUFFER DATA INPUT AS FOLLOWS:

BITS 0-3 ROUTE TO BUFFER ZERO AND BUFFER FOUR
BITS 4-7 ROUTE TO BUFFER ONE AND BUFFER FIVE
BITS 8-11 ROUTE TO BUFFER TWO AND BUFFER SIX
BITS 12-15 ROUTE TO BUFFER THREE AND BUFFER SEVEN

THIS ALIGNMENT CAN EASILY BE DONE BY THE 'POST-FORMAT' REGISTER.

NOW SAY, THE DATA TO BE WRITTEN IS CONTAINED IN BITS 0 TO 3 OF THE 'EMIT' GROUP IN THE PIPELINE, AND WE WANT TO WRITE THIS DATA TO BUFFER ONE, THE FOLLOWING STEPS ARE TAKEN:

1) SET THE POSTFORMAT REGISTER TO 11100000 BINARY/E0 HEX. THIS PLACES BITS 0 TO 3 OF THE ALU LOCAL OUTPUT INTO BITS 0 TO 3 AND 4 TO 7 OF THE ALU DRIVEN OUTPUT, WHICH GOES TO THE EXTERNAL REGISTERS AND THE BUFFER DATA INPUTS.
2) PLACE THE DESIRED BUFFER ADDRESS INTO THE C-ADDRESS REGISTER THROUGH AN ALU OPERATION, SETTING THE C-ADDRESS CONTROL GROUP IN THE PIPELINE TO 'LOAD'. ALTERNATIVELY THE C-ADDRESS UNIT MAY BE CLEARED, INCREMENTED OR DECREMENTED THROUGH THE PIPELINE.
3) ROUTE THE 'EMIT' GROUP TO THE C-DATA REGISTER BY AN ALU OPERATION:
   A) THE ALU A INPUT AT 'EMIT' (NUMBER ZERO).
   B) SET THE ALU TO 'R PLUS CARRY-IN' WITH THE PIPELINE CARRY-IN BIT AT ZERO.
   C) THE ALU OUTPUT SHIFTER AT F TO Y, WITH THE REGISTER FILE AT HOLD, AND THE Q-REGISTER AT HOLD.
   D) THE OUTPUT SELECTOR GROUP POINTING TO THE C-DATA REGISTER (NUMBER ONE).

AT THIS POINT THE BUFFER DATA AND ADDRESS HAVE BEEN PLACED ON THE C BUS, AND THE LAST REMAINING OPERATION, TO DETERMINE THE CONTROL SIGNALS WILL BE DONE THROUGH THE PIPELINE:

4) PLACE THE C CONTROL GROUP TO THESE SETTINGS:
   A) BUS ENABLE(L) AT HIGH
   B) BUFFER ENABLE(L) AT A LOW
   C) BUFFER READ/WRITEE(L) AT LOW
5) WAIT ONE FULL MICRO-INSTRUCTION (200 NANOSECONDS) FOR THE BUFFER TO WRITE THE DATA IN.
   NOTE: THE CONTROL GROUP TAKES EFFECT AT THE BEGINING OF THE MICRO-INSTRUCTION, AND CONTINUES FOR ITS DURATION, WHILE EXTERNAL REGISTERS ARE WRITTEN TO, AT THE END OF A MICRO-CYCLE.

A SAMPLE MACRO-11 PROGRAM THAT SINGLE-STEPS TO READ/WRITE THE BUFFERS IS FOUND UNDER FILENAME:FILERY

LISCNAME: 0
FILENAME: TIMING
UPDATED: 4-AUG-79

T H E T I M I N G O F M I C R O - O P E R A T I O N S

THIS IS A DESCRIPTION OF TIMING OPERATIONS OF THE VIDEO PIXEL PROCESSOR, FROM THE MICRO-PROGRAMS' POINT OF VIEW. ALSO DISCUSSED IS THE INTERCONNECTION IN TIME OF THE BUFFER MEMORIES, OUTPUT REGISTERS AND INPUT SELECTORS. KNOWLEDGE OF THESE RELEATIONSHIPS IN TIME IS CRUCIAL FOR DEVELOPING COHERENT MICRO-PROGRAMS.

THE EMULSIFIER IS THE NAME OF THE COLLECTION OF UNITS, THAT TOGETHER PRODUCE THE IMAGE TRANSFORMATIONS. THESE ARE THE LSI-11 INTERFACE, THE VIDEO PIXEL PROCESSOR, THE IMAGE BUFFERS, THE ADDRESS DISTORTION GENERATOR AND ALL ANCILLARY COMPONENTS TO FACILITATE OPERATION.

THE TIMING FOR THE IMAGE EMULSIFIER IS DERIVED FROM A COMMON CENTRALIZED CLOCK THAT IS LOCKED TO THE HORIZONTAL SYNC PULSE. THIS PHASE LOCKING TO THE HORIZONTAL SYNC ALSO LOCKS TO THE COLOR SUBCARRIER PHASE, IF THE SUBCARRIER IS 'PHASE COHERENT' TO HORIZONTAL SYNC. THIS ALSO IS OF USE WHEN LOCKING TO BLACK AND WHITE SIGNALS WITHOUT A SUBCARRIER, AS WELL AS HETERODYNED TAPE SIGNALS WHERE THE SUBCARRIER PHASE IS UNLOCKED TO HORIZONTAL SYNC. WHEN DEALING WITH TAPE SIGNALS AND TIME BASE ERROR, A SELECTABLE "LOCK RATE" OF SLOW OR FAST MIGHT BE USED TO CORRECT FOR SKEWING OF THE TAPE IMAGE. CURRENTLY A SLOW LOCK IS USED, TRACKING THE AVERAGE RATE OF THE HORIZONTAL SYNC.

THE MAIN CLOCK FREQUENCY IS SET AT 9.75524 MHZ (OPTIONALLY 19.5105 MHZ) WHICH IS AT AN INTEGER MULTIPLE (620 TIMES) THE HORIZONTAL FREQUENCY. THIS HIGH FREQUENCY CLOCK SIGNAL IS FURTHER DIVIDED DOWN BY TWO, ARRIVING AT 4.8776 MHZ, THE MAJOR CLOCK FOR THE IMAGE EMULSIFIER. THIS CLOCK RATE HAS A PERIOD OF 205 NANOSECONDS PER IMAGE CYCLE, THE SMALLEST TIME UNIT FOR INSTRUCTION EXECUTION. INTERNALLY THIS CLOCK IS FURTHER DIVIDED INTO FOUR CYCLES, A T1, T2, T3, AND A T4 CYCLE; EACH OF A 50 NANOSECOND DURATION. THESE FOUR SUBCYCLES CONSTITUTE A 205 NANOSECOND 'MICROCYCLE'.

THE VIDEO PROCESSOR AND IMAGE BUFFERS SHARE THESE MICROCYCLE/MICRO?? TIMING SIGNALS, AND OPERATIONS ARE VIEWED AS OCCURRING AT THE BEGINNING, END, OR DURATION OF A TIMING CYCLE. WE WILL NOW EXAMINE MICROPROGRAM OPERATION, AND RELATE THEIR EXECUTION TO THE TIMING SUBCYCLES (T1, T2, T3, T4), THAT MAKE UP A MICROCYCLE.

PROGRAMMING OF THE VIDEO PIXEL PROCESSOR IS CLOSELY LINKED TO THE TIME SEQUENCING OF INSTRUCTIONS. THE ABILITY TO MICROPROGRAM THE PROCESSOR OPENS OPERATIONS TO PARALLEL EXECUTION, WITHIN ONE MICROCYCLE. THIS PARALLELISM AFFECTS PROGRAM SEQUENCING, ARITHMETIC/LOGICAL FUNCTIONS, BUS ADDRESS AND CONTROL, AND PROCESSOR COMMUNICATION. EACH 'LINE' OF CONTROL CODE CORRESPONDS TO A 'WIDE WORD' OF THE CONTROL STORE. THE OUTPUT OF THE CONTROL STORE IS LATCHED INTO A PIPELINE REGISTER WHICH HOLDS THE BIT PATTERN FOR THE DURATION OF A MICRO-OPERATION. THE OUTPUT OF THE PIPELINE REGISTER IS FURTHER ROUTED TO ENABLE OR ACTIVATE OTHER FUNCTIONS 'HUNG' OFF THE PIPELINE BITS. THESE FUNCTIONAL UNITS MAY BE BROKEN DOWN INTO THE FOLLOWING CATEGORIES:

1) THE MICRO-SEQUENCER
2) ARITHMETIC LOGIC UNIT/REGISTER FILE
3) ALU SELECTED OUTPUTS
4) ALU SELECTED A/B INPUTS
5) THE BUS ADDRESS UNITS
6) THE BUS CONTROL BITS
7) RANDOM NUMBER GENERATOR
8) MULTIPLIER
9) THE IMAGE BUFFERS

EACH UNIT MAY HAVE ITS OWN TIMING PECULIARITIES, BUT THE FOLLOWING OVERVIEW IS HELPFUL:

1) THE MICRO-SEQUENCER

THE SEQUENCER OPERATES AT THE 200 NANOSECOND CLOCK PERIOD. THE PRODUCT OF THE OPERATION OF THE SEQUENCER APPEARS AS THE OUTPUT OF THE PIPELINE REGISTER, AND IS USED TO DETERMINE THE NEXT INSTRUCTION, NEXT TEST CONDITIONS AND NEXT ADDRESS, WHILE THE CURRENT INSTRUCTION IS EXECUTING. THIS ARRANGEMENT IS CALLED A 'ONE LEVEL PIPELINE'. CONDITIONAL INSTRUCTIONS REQUIRE EXAMINATION OF THE TEST BITS. THESE TEST BITS ARE SAMPLED AT THE BEGINNING OF A MICRO-INSTRUCTION. CORRECT OPERATION TESTS THE RESULTS OF A PREVIOUS OPERATION, TO SPECIFY THE CURRENT TEST CONDITIONS. EXTERNAL TEST BITS ARE ALSO SAMPLED AT THE BEGINNING (WITHIN T1) OF A CYCLE. BY THE MIDDLE OF THE MICROCYCLE THE NEXT ADDRESS IS AVAILABLE AT THE SEQUENCER OUTPUT. THE LAST HALF OF THE MICROCYCLE IS USED FOR ACCESS OF THE CONTROL STORE LOCATION, WHICH IS LATCHED AT THE END OF THE CYCLE (THE BEGINNING OF THE NEXT CYCLE).

2) ARITHMETIC/LOGIC UNIT, REGISTER FILE

THE 16 BIT ARITHMETIC LOGIC UNIT CONSISTS OF FOUR MAJOR SECTIONS:

A) DATA INPUT SELECTORS
B) ARITHMETIC LOGIC UNIT
C) A REGISTER FILE
D) OUTPUT SELECTOR
E) STATUS REGISTER

OPERATION OCCURS IN A THREE STEP PROCESS. THE INSTRUCTION IS LATCHED INTO THE PIPELINE REGISTER, MARKING THE BEGINNING OF THE CYCLE. THE DATA INPUTS ARE SELECTED AND ROUTED TO THE ALU SECTION DURING T1. THE ALU PROCESSES THIS DATA FOR THE DURATION OF CYCLE T2 AND T3 WITH THE RESULTS AVAILABLE AT THE END OF T3. THE REGISTER STACK IS WRITTEN TO FOR THE DURATION OF T4 (IF ENABLED BY THE INSTRUCTION). STATUS INFORMATION (NEGATIVE, ZERO, OVERFLOW AND CARRY) IS LATCHED INTO THE ALU STATUS REGISTER AT THE END OF T4 (IF THE STATUS HOLD BIT IS RESET). THE ALU DATA OUTPUT OF THE CURRENT OPERATION IS ALSO MADE AVAILABLE TOWARD THE END OF THE T4 CYCLE.

3) ALU SELECTED OUTPUTS

'EXTERNAL REGISTERS' ARE ENABLED THROUGH USAGE OF THE OUTPUT SELECT GROUP. THESE BITS, WHEN DECODED ENABLE THE APPROPRIATE OUTPUT REGISTERS TO TAKE IN DATA FROM THE ALU DATA OUTPUT. AS THE OUTPUT SELECT GROUP IS A PARTIALLY ENCODED GROUP, ONLY ONE REGISTER MAY BE ENABLED IN A SINGLE MICROINSTRUCTION.

4) SELECTED A/B INPUTS

5) BUS ADDRESS UNITS

IN ITS SIMPLIFIED VERSION, THESE ADDRESS UNITS ARE PRESETABLE UP/DOWN COUNTERS. OPERATIONS OCCUR AT THE END OF THE CURRENT MICROINSTRUCTION, WHETHER IT IS AN UP/DOWN OPERATION, OR LOADING OF THE COUNTER. THE SOURCE FOR LOADING DATA COMES FROM THE OUTPUT OF THE ALU UNIT. WHEN SETTING THE COUNTER TO A VALUE, THE ALU PREPARES THE DATA DURING T1, T2, AND T3 AND ???IS MADE AVAILABLE TO THE COUNTERS DURING T4. THE ACTUAL LOADING OCCURS AT THE END OF T4 OR THE END OF THE CURRENT MICROINSTRUCTION.

6) THE BUS CONTROL BITS

THESE BITS ARE USED TO CONTROL THE STATE OF THE C AND D BUSES. THEY CONTROL THE READ/WRITE LINE AND ENABLE LINES WHICH ARE ROUTED TO THE BUFFERS CONNECTED TO THAT BUS. THESE BITS ARE AVAILABLE AT THE BEGINNING OF THE CURRENT MICROINSTRUCTION (T1) AND ARE MAINTAINED FOR THE DURATION OF THE CURRENT MICROCYCLE.

IT IS USEFUL TO REVIEW THE OPERATION OF THE BUFFERS BY CONTROL OF THESE BITS. FIRST AN ADDRESS IS SET UP IN THE ADDRESS UNIT. ADDRESS UNIT ONE CONNECTS TO THE C BUS, WHILE ADDRESS UNIT TWO CONNECTS TO THE D BUS. ONCE A BUFFER IS ATTACHED TO A BUS THROUGH THE PRIORITY LOGIC OR A SOFT REQUEST, THE CONTROL LINES DETERMINE OPERATION OF THE BUFFER. IF BUFFER ONE IS CONNECTED TO BUS C, A READ OPERATION IS INITIATED AT THE BEGINNING OF A MICROCYCLE, BY SETTING THE READ/WRITE BIT HIGH, AND THE ENABLE BIT LOW. THESE BITS ARE PICKED OFF DIRECTLY AT THE PIPELINE REGISTER AND HENCE ARE AVAILABLE FOR THE DURATION OF THE MICROCYCLE. THE READ OPERATION TAKES A FULL CYCLE AND THE DATA IS AVAILABLE AT THE BUFFER OUTPUT, AT THE END OF THE CURRENT MICROCYCLE. THE WRITE OPERATION REQUIRES SETUP DATA INPUTS AND ADDRESS. ONCE THESE ARE DETERMINED A WRITE OPERATION IS ACHIEVED THROUGH SETTING BOTH THE READ/WRITE AND THE ENABLE BIT TO A LOW. THE WRITE CYCLE OCCURS AT THE BEGINNING OF THE MICROINSTRUCTION AND CONTINUES FOR THE REST OF THE CYCLE. THE 'LOOPED AROUND' DATA IS LATCHED AT THE END OF T4 AND IS AVAILABLE AT THE END OF THE CURRENT MICROINSTRUCTION, AS IS THE OUTPUT FOR READ OPERATIONS.

7) RANDOM NUMBER GENERATOR

8) MULTIPLIER

9) THE IMAGE BUFFERS

SUMMARY

INPUT SELECTION OCCURS AT THE BEGINNING OF A MICROINSTRUCTION, FUNCTIONS AND MEMORY OPERATIONS HAPPEN FOR THE DURATION OF THE MICROINSTRUCTION, AND OUTPUTS ARE WRITTEN TO OR LATCHED AT THE END OF THE CURRENT MICROINSTRUCTION.

DISCNAME: 0
FILENAME: PIXEL
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PROGRAMMING OF THE VIDEO PIXEL PROCESSOR

THIS IS A DISCUSSION OF METHODS AND TECHNIQUES, FOR WRITING EXECUTABLE MICROPROGRAMS, FOR PROCESSING OF BUFFER MEMORIES AND OTHER RELATED PROGRAMMABLE UNITS.

THE VIDEO PIXEL PROCESSOR IS A HIGH SPEED BIPOLAR MICROPROCESSOR, OPERATING AT A CYCLE TIME OF 200 NANOSECONDS. IN A SINGLE CYCLE AN INSTRUCTION CAN BE EXECUTED, RESULTING IN CONTROL OF MANY OPERATIONS IN PARALLEL. THE NUMBER OF UNITS THAT MAY BE CONTROLLED IS DETERMINED BY THE WIDTH OF THE CONTROL WORD. EACH CONTROL WORD IS SUBDIVIDED INTO 'FIELDS' OR CONTROL GROUPS, WHICH INDEPENDENTLY CAN BE CONNECTED TO DIRECT OPERATION OF OTHER FUNCTIONAL UNITS.

PROGRAMS ARE WRITTEN INTO A PROGRAM STORE, SO CALLED WRITABLE CONTROL STORE, WHICH HOLDS THE CONTROL FIELDS OR GROUPS. THE CONTROL STORE IS FIRST FILLED WITH THE DESIRED PROGRAM OF CONTROL GROUPS, THEN STEPPED THROUGH BY THE MICRO-PROGRAM SEQUENCER. THE MICROPROGRAM SEQUENCER ACTS AS A PROGRAM COUNTER TO 'PICK' ITS WAY THROUGH THE PROGRAM CONTROL STORE. THE OUTPUT OF THE CONTROL STORE IS ROUTED THROUGH A PIPELINE REGISTER, WHICH HOLDS THE CURRENT MICROINSTRUCTION FOR THE DURATION OF A MICROINSTRUCTION CYCLE. THIS MICROINSTRUCTION IS MERELY THE COLLECTION OF CONTROL GROUPS THAT 'STEER' THE OTHER FUNCTIONAL UNITS 'HUNG' OFF THIS PIPELINE REGISTER. THE SEQUENCER ITSELF IS PARTIALLY INSTRUCTED BY THE CURRENT PIPE-LINE REGISTER, TO DETERMINE ITS NEXT INSTRUCTION, TO STEP THROUGH THE CONTROL STORE.

THE PIPELINE REGISTER IS DIVIDED INTO SIX MAJOR CONTROL GROUPS WHICH CONTROL:

1) THE MICROPROGRAM SEQUENCER
2) A GENERAL PURPOSE 16 BIT EMIT GROUP
3) THE ARITHMETIC/LOGIC UNIT, REGISTER STACK AND EXTERNAL REGISTERS
4) THE TWO ADDRESS FORMATION UNITS
5) THE CONTROL LINES FOR THE MEMORY BUFFER ON THE C- AND D- BUSES
6) RANDOM NUMBER GENERATOR
7) EXTRA CONTROL GROUP FOR ADDITIONAL SUPPORT CIRCUITS

WE WILL NOW EXAMINE IN GREATER DETAIL EACH CONTROL GROUP, WHAT THEY CONTROL AND THE ASSEMBLAGE OF THESE GROUPS TO MAKE UP MICROPROGRAMS FOR BUFFER, IMAGE AND AUDIO TRANSFORMATIONS:

DISCNAME: X
FILENAME: TESTS.DOC
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TESTING THE VIDEO PIXEL PROCESSOR

OUTLINED IS A STEP BY STEP PROCEDURE FOR DIAGNOSING HARDWARE MALFUNCTIONS IN THE IMAGE EMULSIFIER. SOME OF THESE TESTS REQUIRE MONITORING WITH A DUAL CHANNEL OSCILLOSCOPE, TO VERIFY PROPER OPERATION. TEST PROGRAMS ARE SUPPLIED WHERE POSSIBLE, AND SIMPLIFY ERROR DETECTION. THE LIST IS ORDERED TO OUTLINE A RECOMMENDED STEP BY STEP INVESTIGATION WHEN HARDWARE ERRORS ARE SUSPECTED. NOTE THAT SOME ERRORS ARE NOT DETECTEABLE UNDER PROGRAM CONTROL. THESE ARE MAINLY DEFECTS IN SYSTEM TIMING CAUSED BY DEFECTIVE CIRCUITS, WHICH CAN BE POINTED TO ONLY UNDER FULL SPEED OPERATION. THESE PROGRAMS DO DETECT STATIC PROBLEMS, MISTAKES WHICH ARE CAUSED BY WIRING ERRORS, AND MAJOR FAILURE IN INTEGRATED CIRCUITS. THE BEST TEST OF THE EMULSIFIER IS ITS OPERATION UPON KNOWN IMAGE DATA, AT FULL SPEED.

TEST SEQUENCE

1) TEST POWER SUPPLY AND CHECK FOR PLUS FIVE VOLTS ON DIGITAL RACK
2) VERIFY THAT THE LSI-11 INTERFACE IS CORRECTLY INSTALLED IN BACKPLANE (CORRECT SLOT) AND THAT THE INTERFACE CABLE SUCCESFULLY REACHES THE DIGITAL RACK ON THE BOTTOM SLOT(S1-J3)
3) TEST LSI-11 INTERFACE - DOES IT ADDRESS (NO M-TRAPS)
4) TEST LSI-11 MICRO-REGISTER DECODERS
   - A) READ DECODERS
   - B) WRITE DECODERS
5) CHECK WRITING AND READING OF THE LSI-11 'FORCE-ADDRESS' REGISTER.
6) TEST FORCE-ADDRESS BIT, AND FORCE-ADDRESS SELECTORS
7) TEST CLOCK
   - A) MASTER X CLOCK
   - B) UNGATED ALU/SEQUENCER CLOCK
   - C) RUN/HALT THE GATED CLOCKS
   - D) SINGLE STEP THE PIPELINE CLOCK
   - E) SINGLE STEP THE ALU GATED CLOCK
8) CONTROL STORE / PIPELINE TEST
9) TEST ALU SELECTOR DECODERS
   - A) A INPUT SELECTOR DECODERS
   - B) B INPUT SELECTOR DECODERS
   - C) OUTPUT SELECT DECODERS
10) TEST EMIT TO ALU TO READBACK TEST
11) TEST A INPUT SELECTORS - EMIT TO ALU READBACK
12) TEST ALU EXTERNAL REGISTERS, A INPUT SIDE
13) TEST B INPUT SELECTORS - EMIT TO ALU READBACK
14) TEST ALU EXTERNAL REGISTERS, B INPUT SIDE
15) CHECK SEQUENCER OPERATION
16) CHECK ARITHMETIC/LOGIC UNITS (ALU) OPERATION
17) TEST THE IMAGE BUFFERS ON THE A,C,D BUSES
18) READ OUT THE BUFFERS TEST PATTERN WRITTEN BY STEP 17 TO THE VIDEO SCREEN USING THE B-BUS (THE ADDRESSING BOARD)
19) TEST THE EXTERNAL B-DATA FRAME-GRAB INPUT FOR CORRECT 'REAL-TIME' ACQUISITION OF AN IMAGE, USING THE READ-VERIFY-WRITE MODE OF THE ADDRESSING BOARD
20) CHECK CORRECT OPERATION OF ADDRESS UNIT ON THE ADDRESSSING BOARD
   - A) THE STANDARD X-Y SCAN
   - B) THE 'SCREEN-OFFSET' REGISTERS (THE 'SHIFT' FUNCTION)

DISCNAME: X
FILENAME: BRAKUP.DOC
UPDATED: 5-DEC-79

BOARD BREAKDOWN - FUNCTIONAL BLOCKS

1) ALU/SEQUENCER BOARD
   A) ARITHMETIC LOGIC UNITS
      1) ARITHMETIC LOGIC UNITS: AMD 2903 ALU0-3
      2) LOOK-A-HEAD CARRY UNIT: AMD 2902 LCAR
      3) STATUS LATCH/COND.TEST SEL.: AMD 2904 STMUX
   B) SEQUENCER/CONTROL STORE/PIPELINE
      1) CONTROL STORE
         A) WRITABLE CONTROL STORE - 256 WORDS BY 80 BITS: FAIRCHILD 93L422
         B) BANK DECODER
      2) PIPELINE REGISTER - 80 BITS WIDE: AMD 25S18
      3) SEQUENCER
         A) SEQUENCER/CONTROLLER: AMD 2910
         B) 'DIRECT' EMIT GROUP DRIVER
         C) TEST/STATUS MULTIPLEXER: AMD 2920
         D) FORCE ADDRESS SELECTOR
   C) LSI-11 MICRO-REGISTERS
      1) LSI-11 ADDRESS DECODING LOGIC
      2) MICRO CONTROL/STATUS REGISTER
      3) ALU READBACK REGISTER
      4) LSI-11 MICRO-ADDRESS REGISTER
      5) SEQUENCER MONITOR REGISTER
      6) ALU MONITOR REGISTER
   D) CLOCK GATING LOGIC
      1) MICRO-CONTROL/STATUS REGISTER
         A) HALT, SINGLE STEP LATCHES
         B) SINGLE STEP ENABLE BITS - PIPELINE AND ALU
         C) MEMORY TRAP LATCH
   E) EXTERNAL ALU REGISTERS
      1) C-DATA REGISTER
      2) D-DATA REGISTER
      3) C-ADDRESS REGISTER
      4) D-ADDRESS REGISTER
      5) PRESELECT A LATCH
      6) PRESELECT B LATCH
      7) POSTFORMAT LATCH
   F) POSTFORMAT / ALU OUTPUT DRIVER
      1) POSTFORMAT SELECTOR
      2) ALU OUTPUT DRIVER